Kenichi Okada · Shouhei Kousai
Editors

Digitally-Assisted Analog and RF CMOS Circuit Design for Software-Defined Radio

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Preface

Software-defined radios (SDRs) that are capable of transmitting and receiving modulated signals in any frequency band have long been desired. They are very attractive, especially as mobile devices, since mobile devices need to be compact even if they are compliant with many different wireless standards. In fact, recent mobile devices are required to offer an enormous range of wireless standards (e.g., 2G/3G/3.5G/3.9G/4G cellular, WLAN/WPAN, GPS, broadcasting).

For many years, various aspects of SDRs have been investigated and many technologies for realizing SDRs have been developed. However, it is still difficult to realize a practical SDR device. This is mainly because conventional RF front ends are not sufficiently flexible to satisfy the requirements for all modulation schemes and frequency bands. SDR transceivers must satisfy quite a diverse range of requirements depending on the wireless standard. For example, the frequency bands required are widely spread between 400 MHz and 6 GHz. On the other hand, SDR transceivers are also required to have competitive performances (in terms of power consumption, sensitivity, etc.) with those of other single-band transceivers.

A key idea for realizing SDR transceivers has recently been proposed: digitally assisted analog and RF circuits. Many circuit applications that use this concept have been reported and they are highly flexible. Thus, SDR transceivers are fairly close to becoming a reality. This book introduces potential circuits for SDRs, including RF, analog, and mixed-signal circuits.

This book is based on recent research conducted by the authors. It discusses approaches for realizing SDR transceivers using recently developed advanced CMOS technology, which use millions of fast transistors. One of the most important technologies for realizing SDR transceivers is a design technique of *digitally assisted analog and RF circuits* since SDR transceivers require high flexibility and programmability. This book covers every circuit block available for SDR transceivers to illustrate the various applications of digitally assisted circuits.

The book is aimed at graduate students who are designing CMOS wireless transceivers as well as professional circuit designers and researchers of wireless systems, antenna, and other wireless components. It assumes a basic knowledge of analog and RF circuit design and covers the entire transceiver, including the receiver,

transmitter, local oscillator, analog baseband, ADC, and DAC. Each chapter stands alone so that readers can select topics that interest them. Chapter 1 provides a brief overview and describes the relationships between the other chapters. The subsequent chapters are organized as follows:

Chapter 2 was written by Jan Craninckx of IMEC in Belgium. It describes a transceiver front-end for a SDR, which contains a quadrature local synthesizer and a 25%-duty sampling mixer. This transceiver is even capable of SAW-less FDD operation. It is one of the most promising SDR front-ends, and it should be considered by every SDR researcher.

Chapter 3 was written by Robert Bogdan Staszewski of Delft University of Technology in the Netherlands. It describes the key concepts of digital RF and digitally assisted RF circuits, including an all-digital PLL and a direct-sampling mixer, which are now essential components for highly integrated CMOS transceivers.

Chapter 4 was written by Rahim Bagheri of Wilinx Corp., Ahmad Mirzaei and Saeed Chehrazi of Broadcom Corp., and Asad A. Abidi of the University of California in Los Angeles, California. It describes the first practical SDR receiver, which represents a historic achievement and indicates the direction of future SDR research.

Chapter 5 was written by Eric Klumperink, Zhiyu Ru, Niels Moseley, and Bram Nauta from the University of Twente in the Netherlands. It describes a practical SDR receiver that uses digitally enhanced harmonic rejection for robustness against interference.

Chapter 6 is written by Masaki Kitsunezuka, NEC Corp.; Shinichi Hori, NEC Corp.; and Tadashi Maeda, Renesas Electronics Corp., Japan. This chapter describes a tunable LPF that uses duty-cycle control of an analog baseband.

Chapter 7 is written by Akira Matsuzawa of the Tokyo Institute of Technology in Japan. It discusses reconfigurable data converters, focusing especially on a delta-sigma analog-to-digital converter that can be used to realize both a tunable resolution and a tunable conversion speed.

Chapter 8 is written by Shouhei Kousai of Toshiba Corp. This chapter describes a flexible, highly efficient, watt-level transmitter. This work was conducted by the Caltech High-Speed Integrated Circuits Group (CHIC).

We would like to acknowledge the chapter authors for their enormous effort in helping to prepare this book. They devoted considerable time to this book, even during their precious holidays. It would have been impossible to publish this book without their full cooperation.

Each chapter was subjected to a rigorous review process. We would like to thank the many volunteer reviewers for their insightful and constructive comments including Yohei Morishita (Panasonic Corp.), Masaki Kanemaru (Panasonic Corp.), Jun Deguchi (Toshiba Corp.), and some anonymous reviewers.

Finally, we would like to thank Charles Glaser and Elizabeth Dougherty of Springer for their generous and ongoing support and guidance.

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Contents

1 Introduction 1
Shouhei Kousai

2 Nanoscale CMOS Transceiver Implementation for a Software-Defined Radio Platform 3
Jan Craninckx

3 Digital RF and Digitally-Assisted RF 35
Robert Bogdan Staszewski

4 Software-Defined Radio Receiver Architecture and RF-Analog Front-End Circuits 85
Rahim Bagheri, Ahmad Mirzaei, Saeed Chehrazi, and Asad A. Abidi

5 Interference Rejection in Receivers by Frequency Translated Low-Pass Filtering and Digitally Enhanced Harmonic-Rejection Mixing 113
Eric Klumperink, Zhiyu Ru, Niels Moseley, and Bram Nauta

6 Reconfigurable Analog Baseband Filter 151
Masaki Kitsunezuka, Shinichi Hori, and Tadashi Maeda

7 Multi-Standard Data Converters 171
Akira Matsuzawa

8 Highly Linear and Efficient Watt-Level SDR Transmitter with Power Mixer Array 191
Shouhei Kousai

Index 217

Chapter 1
Introduction

Shouhei Kousai

The aim of this book is to assist with developing software-defined radio (SDR) transceivers and their related circuit techniques in CMOS. The book is structured as follows.

Chapter 2 describes a practical CMOS implementation of an SDR transceiver. It can transmit and receive signals of commonly used wireless communication standards in a frequency range of 0.1–6.0 GHz. It contains several low-noise amplifiers, driver amplifiers, and local oscillators to cover this frequency range and their performance is critical to the transceiver. The class-C VCO described in this chapter has a trade-off between noise and power consumption, offering the flexibility required for an SDR transceiver. The other circuit blocks (i.e., IQ up-conversion and down-conversion mixers and an analog baseband (ABB)) are highly tunable, enabling them to accommodate multiple standards in a single circuit block. The performance of the SDR transceiver is competitive with or even better than that of a transceiver designed for a single wireless standard.

Chapter 3 describes a digital RF transceiver that has the most important characteristics for an SDR transceiver: programmability and flexibility. The key concepts of digital RF transceivers, such as all-digital PLL (ADPLL), discrete-time analog signal processing, digital-to-frequency converter (DFC), and digital-to-RF amplitude converter (DRAC), are explained in detail. This chapter emphasizes the advantages of time-domain signal processing over conventional voltage or current-domain signal processing in scaled CMOS technology in terms technical, historical, and commercial aspects.

An advanced SDR receiver is discussed in Chap. 4. The basic concept is to remove the RF-front-end filters (i.e., SAW filters) and to increase its flexibility so that it can accommodate future wireless standards. Strong out-of-band blockers can be rejected by employing the combination of a rectangular window integration

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sampler, a discrete-time analog infinite impulse response (IIR) filter, and a discrete-time analog decimation filter (DTDec); this configuration exploits the highly flexible and programmable discrete time analog signal processing introduced in Chap. 3. Wideband noise cancelling LNA operating from 800 MHz to 6.0 GHz with a noise figure (NF) of less than 2.5 dB is demonstrated. It employs a common-gate (CG) and common-source (CS) amplifier and can provide a balanced output without an off-chip balun. An harmonic rejection (HR) mixer is also described for rejecting third and fifth harmonic mixing, which is a major challenge in wideband transceivers.

The above-mentioned challenges of harmonic mixing and out-of-band blocker rejection are further discussed in Chap. 5. In a wideband SDR receiver, an out-of band blocker can be much stronger than in-band blockers, since the RF-front end does not provide blocker rejection (unlike in conventional receivers). This chapter explains a receiver front-end architecture for maximizing the blocker immunity while maintaining a high sensitivity. The blocker is rejected before the first high-impedance node, thus preventing intermodulation. This chapter also describes two harmonic rejection (HR) techniques: an analog two-stage polyphase HR and digitally enhanced HR. Without any calibration, the analog HR achieves a rejection of more than 60 dB and mismatch robustness. The digitally enhanced HR achieves an even better rejection of over 80 dB.

The major advantages of the discrete-time filtering discussed in Chaps. 3 and 4 are its high rejection obtained by zero insertion and frequency tunability. These advantages are fully exploited to realize a reconfigurable analog baseband (ABB), which is described in Chap. 6. A duty-cycle-controlled discrete-time transconductor combined with an op-amp integrator is introduced. It allows the poles and Q of a second-order LPF to be tuned almost arbitrarily. Passive LPF and four-tap FIR filter, which can be buried in the second-order LPF, can solve the problem of *aliasing*. Tunability of the cut-off frequency from 400 kHz to 30 MHz and Butterworth, Chebyshev, and elliptic filter transfer functions are demonstrated.

Chapter 7 reviews data converters for SDR transceivers, focusing especially on delta-sigma analog-to-digital converters (ADCs). Their high resolutions permit channel selection in the digital domain and thus enable high programmability and flexibility. They also offer a trade-off between power consumption and bandwidth, which can realize a comparable performance with ADCs designed for a single standard. Previously published ADCs are analyzed and are compared in terms of bandwidth, signal-to-noise ratio (SNR), technology node, topology, and power dissipation. This reveals the design requirements and limitations for a multimode ADC.

Chapter 8 describes a power mixer array as an efficient and flexible power generation approach for CMOS. The concept of digital power amplifier (DPA) described in Chap. 3 is expanded to transmit a watt-level modulated signal and to reject an aliasing signal, while maintaining the programmability of DPA. It comprises several power mixer units that are dynamically turned on and off to enhance the linearity and back-off efficiency. At the circuit level, the power mixer unit can operate as a switching amplifier to achieve a high peak power efficiency.

Chapter 2
Nanoscale CMOS Transceiver Implementation for a Software-Defined Radio Platform

Jan Craninckx

A Software-Defined Radio (SDR) should theoretically receive and transmit any modulated frequency channel in the (un)licensed spectrum, targeting all modern communication standards relevant for a modern handheld mobile device (2G/3G/4G cellular, Wireless Local Area Networks (WLAN), Bluetooth, Global Positioning System (GPS), broadcasting, etc.). Moreover, it should guarantee top performance with energy savings, while still being integrated in a digital CMOS technology. In this chapter, a practical front-end implementation for such an SDR concept is demonstrated, including local oscillator, transmitter and receiver in the frequency range 0.1–6 GHz. Circuits and architectures are optimized for minimal area occupation in a standard digital 40 nm low-power (LP) CMOS technology. The radio front-end compares favorably with state-of-the-art dedicated radios while enabling, for the first time, wideband reconfigurable performance and energy scalability.

2.1 Introduction

Driven by increasingly sophisticated user demands, wireless communication systems are moving towards an era where ubiquitous connectivity and growing levels of integration will be essential for most applications. This wireless revolution will not slow down in its penetration of society for the foreseeable future. There is on the one hand a market pull by an increasingly connected world population asking for vast information resources through the internet and/or mobile phones. On the other hand, there is a market push from a hundreds of billions dollar industry delivering all kinds of communication products and applications. In this context, mobile handsets can

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represent a real bottleneck as they incorporate several concurrent constraints (e.g., in battery duration, cost, performance, size, weight) that compromise the flexibility of future networks.

Although the most advanced smart phones already support an increasing number of radios, convergence of standards is currently achieved by simply assembling dedicated ICs on ultradense printed circuit boards (PCBs), which can finally turn into a significant increase in component count and Bill of Materials (BoM). System-on-Chip (SoC) solutions have also appeared, which integrate multiple RF front-ends and modems on the same chip, mostly relying on digitally assisted design techniques. However, current focus is still on the selection of a few limited standards having very similar requirements. Moreover, most of these transceivers provide state-of-the-art performance at fixed power levels whereas in many scenarios, tens of mWs could still be saved by tuning the radio at run-time, based on actual communication conditions [1].

We believe that the road to a *universal radio* lies in all-CMOS designs based on agile analog front-ends and a Software-Defined Radio (SDR) platform. Clearly enough, the original Software Radio (SR) concept [2], featuring a high dynamic range ADC able to *concurrently* receive any possible frequency channel directly at the antenna, remains still unrealistic for battery-powered devices. On the other side, an SDR device, whose key performances are configurable by software and which supports the reception/transmission of several standards (one-at-a-time) proves to be a pragmatic approach, which can bring significant advantages, ranging from lower BoM to universal RX/TX capabilities and considerable energy savings [3–5].

The mobile terminal that delivers the ultimate user experience will require a Software-Defined Radio (SDR) platform as the one depicted in Fig. 2.1. It consists of multiple front-end modules, possibly leveraging heterogeneous and 3-D integration technologies, a digitally assisted analog front-end and a reconfigurable base-band engine [6], both integrated in a digital nanometer CMOS technology. It is capable of transforming itself satisfying the requirements of any desired communication protocol while still providing competitive power consumption. A software *brain* is also present to guarantee advanced quality of service (QoS) and best power/performance trade-offs at any time via a cross-layer approach, since measuring performance requires taking into account the characteristics of the protocol stack, whereas optimizing energy expenditure assumes detailed knowledge of the low-level radio hardware [1].

The need for a reconfigurable radio front-end is already visible with the advent of Long Term Evolution (LTE) [7], where one of the key technical aspects is the large flexibility that is required from the radio front-end. Indeed, LTE combines variable baseband bandwidths with variable RF frequencies. As a result, a Software Defined Radio platform is the perfect base for an LTE front-end, as it provides the needed flexibility while offering tunable power/performance trade-offs.

As data rate requirements continue to increase, several communication standards will extensively use multiple transceiver branches (like multiple-input and multiple-output (MIMO)) in order to fit the required data rate (Mbit/s) in the pricy and thus limited available spectral bandwidths (MHz). Again, multiplying dedicated

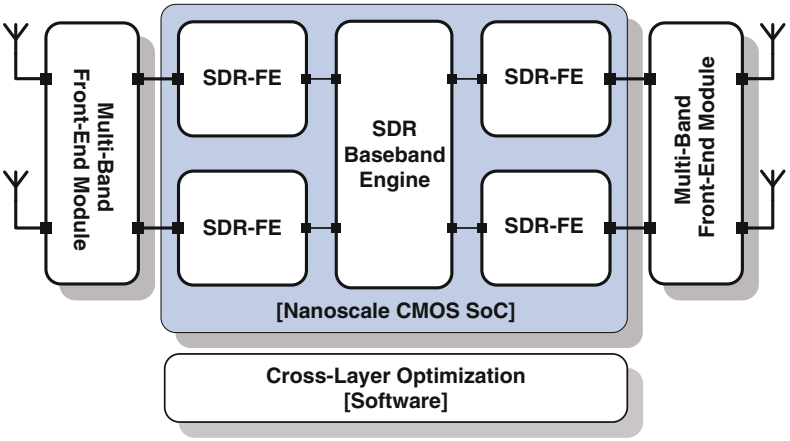

Fig. 2.1 The possible instantiation of the ultimate SDR platform includes 4+ coexistent Software-Defined radio front-ends and a powerful baseband engine all integrated in a nano-scale digital CMOS technology. Energy and spectrum awareness is guaranteed by cross-layer optimizer whereas initial band selection and power amplification is provided by multi-band front-end modules

hardware for this increases cost and size, whereas a mobile terminal that consists of a few SDR hardware instantiations, as shown in Fig. 2.1 could be the ideal solution for this. In the usual operating mode, the radios can keep the user connected to a few systems, e.g. one cellular system, one for connectivity and one for broadcasting reception. At data rate peaks, these SDRs could all be programmed into a high-capacity MIMO mode for e.g. an 802.11n or an LTE-Advanced system for a limited amount of time, thus implementing all desired user functionality at minimal hardware cost. Note that in the proposed scheme, functionality and complexity of the system are not correlated. A commercial range of handheld devices could be differentiated by the number of SDR front-ends in the device. High-end devices would contain many front-ends and would be able to provide many services concurrently (e.g. broadband *and* cellular *and*…). The lowest end devices could have only one SDR front-end, which would limit the connection to one at a time, still to be chosen out of many standards (e.g. broadband *or* cellular *or*…).

Another 'powerful' aspect of an SDR platform is its energy awareness. The user's data does not have to be transmitted over the single protocol a dedicated terminal might be equipped with. Instead, the most optimal link can be chosen that enables the smallest required energy per bit, or maybe the one where the subscription cost is the lowest. Also within a certain communication link, the channel conditions may be such that the power budget can be optimized by reprogramming the hardware in the best trade-off for noise, filter order, linearity, etc. while still meeting all regulations for that standard. These trade-offs that are traditionally done only during the design phase of the radio, are now also possible at run-time, allowing for the best compromise possible between user experience and battery life.

A final example of the use of SDR would be the ability of the terminal to 'upgrade' itself by downloading a new configuration that allows it to be reconfigured into a new operating mode compatible with a new upcoming standard.

This chapter describes the implementation of a prototype radio front-end transceiver that follows this SDR concept [4,5], targeting all modern communication standards relevant for a modern handheld mobile device. In order to be accepted by the market as a possible solution, all the required flexibility should come at (almost) no cost, and performance should be similar to dedicated implementations. For a cost-effective implementation as part of the radio System-on-Chip (SoC) that will be dominated by a complex digital processor, the chosen technology is the most advanced one available today, i.e. 40 nm LP digital CMOS without any analog/RF option. The rest of this chapter is organized as follows. Section 2.2 describes the choices made on the architecture of the transceiver front-end. More details on the frequency synthesis, the receiver and the transmitter are given in Sects. 2.3, 2.4 and 2.5, respectively. Section 2.6 reports the measurement results and finally in the last section some conclusions are drawn.

2.2 SDR Architecture

As shown in Fig. 2.2, we leverage a reconfigurable Zero-IF architecture, which has shown the highest potential to reduce costs, size and power, even under flexibility constraints [8, 9]. Only modes with a very low bandwidth (such as e.g. GSM) will use a low (half-channel) IF frequency in receive mode to limit the impact of flicker noise. Although concurrently handling a few wireless standards may be a desirable feature in the future, we reasonably assume that this is a very unlikely scenario for the majority of mobile users at the moment, and hence are able to limit the major constraints and challenges in the design of the radio budget and the associated circuit blocks to those also present in single-mode radios.

As this SDR front-end needs several hundreds of control bits, a scalable Network-on-Chip (NoC) [10] is implemented to allow configuring each analog block, monitor the front-end performance, and dynamically control its behavior. To obtain state-of-the-art performance over a wide range of carrier frequencies and bandwidths, we rely on the advantages of a scaled technology together with adequate circuit design techniques and extensive calibration [11, 12]. To further reduce silicon area we limit the use of bulky passive components such as high-Q inductors, and adopt a proper distribution of gain stages. For example, increasing the gain (and the gain steps) as early as possible in the RX chain can relax the noise specifications of the baseband section and consequently yield a decrease in capacitors sizes and power consumption. However, this also implies tougher linearity requirements.

To allow frequency-division duplex (FDD) operation, the transceiver contains two high-frequency fractional-N phase-locked loops (PLLs). Both RX and TX PLLs leverage a high-band (HB) and low-band (LB) voltage-controlled oscillators (VCOs) that cover an uninterrupted range from 6 to 12 GHz, with adjustable VCO

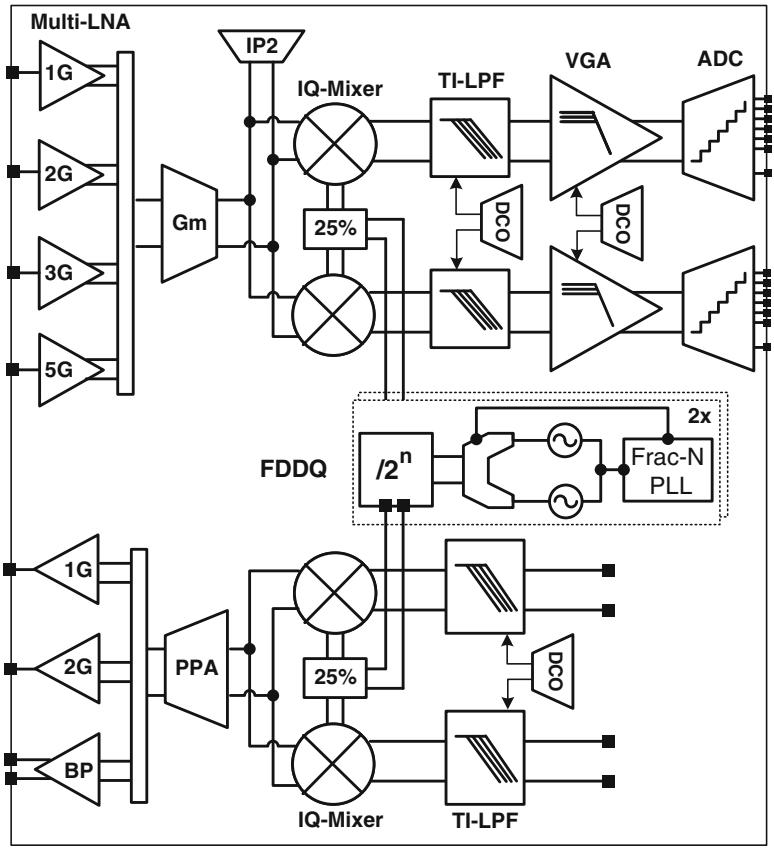

Fig. 2.2 SDR Block diagram

gain. The high frequency of operation lowers pulling effects, and yields low area consumption for the VCOs. Local oscillator (LO) synthesis for all RF frequency bands below 6 GHz can therefore be provided by plain division-by-2^N, which is implemented with a chain of full-swing CMOS dynamic dividers.

On the receiver side, a difficult choice to make is the number of low-noise amplifiers (LNA) to be used. While adding a separate LNA for each targeted frequency band can bring too much area overhead, having one single wideband LNA that covers the full 0.1–6 GHz RF input range is also not optimal. Although such an LNA has already been demonstrated [13], it might show some noise/gain limitations at the edge of the RF band, it will not provide any attenuation of far-away blockers so increasing the system's linearity requirements. Also, the total system will also suffer some extra losses due to interfacing issues with an array of fixed antenna filters (that will still be needed to block heavy out-of-band blockers). Therefore, the compromise of using four LNAs has been chosen here, targeting each a sufficiently wide frequency band to cover the full range up to 6 GHz.

The rest of the receive chain is constructed out of a 25% duty cycle passive mixer, a fifth order baseband trans-impedance low-pass filter (TI-LPF), a variable-gain amplifier (VGA) and a low-power 10-bit 60 MS/s successive approximation (SAR) analog-to-digital converter (ADC). Mixed-mode calibration is used for second order intermodulation and DC offset. This will be further detailed in Sect. 2.4.

The transmitter chain starts with a programmable third order reconstruction filter that removes digital-to-analog converter (DAC) aliases. For low out-of-band noise, which is a crucial performance requirement in most FDD standards, a 25% duty cycle passive voltage sampling mixer is used [14]. The RF section consists of a triple-band pre-power amplifier (PPA) with integrated transformer baluns.

2.3 Frequency Synthesis

While still adopting a "classical" analog architecture, the frequency synthesizer couples multi-mode programmability with design techniques exploiting the speed capabilities of the scaled digital technology and limiting the area overhead due to passive devices. Indeed, many wideband frequency synthesis architectures must rely on poly-phase filters, multiplication, or single-side band (SSB) mixing [7] to achieve the required range of carrier frequencies desired in an SDR. However, all these techniques may easily become power-hungry and yield undesired spurious tones. In 40-nm CMOS, a fundamental VCO frequency up to 12 GHz is possible because of the intrinsically higher speed of the technology, and hence we propose to generate the LO quadrature signals by starting from a high-frequency LC-VCO signal and cascading divide-by-2 circuits [15].

A full octave tuning range (6–12 GHz) is needed to generate quadrature LO at all frequencies below 6 GHz. This is not possible with a single VCO, but two parallel VCOs centered at different frequencies can cover this range. Since at these high frequencies only small inductors are used, the area overhead is also limited. Therefore, a dual-VCO, fourth order, type-2 $\Sigma\Delta$ fractional-N PLL is implemented at the heart of our frequency synthesizer. The two VCOs cover the 6–12 GHz bandwidth while low-complexity cascaded divide-by-2 cells are used to generate quadrature frequencies. All building blocks can be programmed to achieve different carrier frequencies, VCO sensitivities, loop bandwidths, phase noise values and power consumptions.

2.3.1 Reconfigurable PLL

The simplified block-diagram of the reconfigurable PLL is represented in. The phase-and-frequency detector (PFD), which is robust to crossover distortion, implements a programmable dead-zone delay between 0.86 ns and 1.55 ns to allow fine tuning for different charge pump current settings. The charge pump (CP) leverages

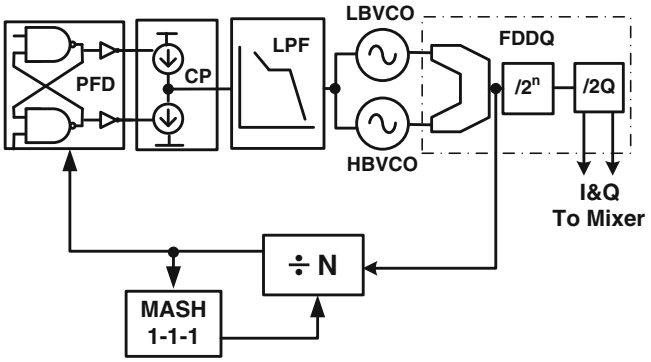

Fig. 2.3 Simplified block diagram of the ΣΔ frequency synthesizer

eight parallel replica-biased current units and allows for up to 1.5% mismatch compensation. The CP current, programmable between 45 and 360 µA, is fed into the low impedance input of a third order reconfigurable active-RC filter. While keeping the total amount of capacitance constant (approximately 200 pF), the filter configures its resistors to allow for cross-over frequency tuning between 110 and 320 kHz.

Based on the targeted frequency, either the 6–9 GHz low-band (LB) or the 9–12 GHz high-band (HB) VCO is active, whose output signal is selected by a high-speed CMOS multiplexer that drives the PLL frequency divider and the frequency distribution and division-in-quadrature circuit (FDDQ), which generates LO signals in the 0.1–6 GHz band. With a reference crystal of a few tens of MHz, a divider with a wide programmable range, e.g. from 128 to 511, is needed to close the loop of the PLL (Fig. 2.3).

2.3.2 LC Voltage Controlled Oscillators

Both VCOs adopt the class-C single-NMOS differential-pair topology [16] represented in Fig. 2.4 With respect to a standard LC-VCO, this topology produces a larger oscillation amplitude for a given bias current, potentially leading to improved phase noise performance for a given power budget. In fact, rather than operating as switches, the NMOS transistors in this topology either act (prevalently) in the active (saturation) region or they are off. As a consequence, the contribution of the core transistors to phase noise is basically as low as in the standard LC-VCO, but the amplitude of the fundamental current harmonic is maximized, as in a Colpitts oscillator, finally producing a net improvement of 3.9 dB for the same power consumption, and of 6 dB for the same oscillation amplitude. Additional advantages include built-in filtering of noise from the tail current source and lower sensitivity to stray capacitances at the common source node.

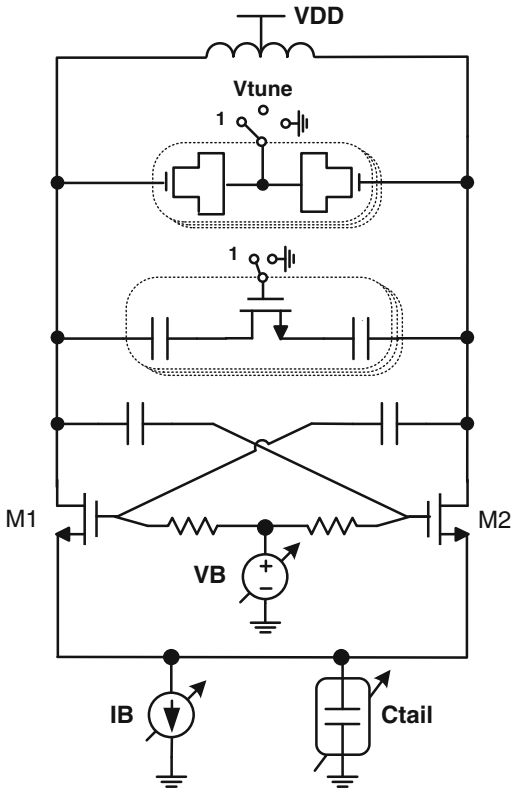

Fig. 2.4 The class-C LC-tank voltage controlled oscillator

However, to guarantee class-C operation in the current limited regime, the maximum oscillation amplitude offered by a class-C VCO is always lower than the one of a standard LC-VCO. In fact, to operate the transistors in saturation, the output amplitude will be limited by $A_{max} = V_{DD} - V_B + V_{Tn}$ where V_B is the transistor gate bias voltage and V_{Tn} is the threshold voltage. To achieve higher oscillation swings and overcome this limitation, we program V_B and I_B to allow the MOS devices to operate in moderate inversion (as far as the oscillation startup condition is met) and even moderately enter the triode region when needed. Proper device biasing is crucial to optimize noise performance, since variations of 100–200 mV in V_B may cause a sensible increase in phase noise. In our implementation, a 4-bit DAC, ac-coupled with the gates of the transistor pair, generates a gate voltage value in 50-mV steps.

In both VCOs, the tank inductor is a center-tapped single turn horseshoe coil, drawn in the topmost metal, shunted with the superficial aluminum redistribution layer. In fact, low phase noise values, for a given tank amplitude, call for larger tank capacitance and smaller inductance (0.4 nH in our case) based on analysis in [16]. A small inductance value is also preferred to increase the tuning range.

We use coarse frequency tuning to split a large tuning range into smaller bands. This allows covering our range of interest without increasing the VCO sensitivity

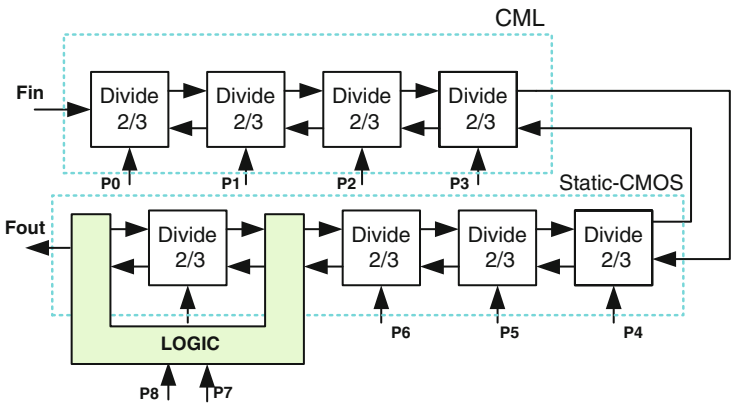

Fig. 2.5 Enhanced range divider supporting seamless ΣΔ divide modulus dithering

K_{VCO}, which would increase the level of the PLL spurs and phase noise. Coarse frequency band selection is done with a 6-bit low-cost MoM capacitor array. Within each band, the tank capacitance is then finely tuned through an array of 15 differential NMOS varactors. These varactors can be switched on or off for fine band selection, or connected to the tuning voltage V_{TUNE} to control the VCO gain for optimal PLL design [17]. For instance, K_{VCO} can be programmed to linearly scale with the PLL frequency to provide constant bandwidth.

Each VCO can further trade performance for power consumption, by also adjusting the bias current, the gate bias voltage, as well as the tail capacitance C_{tail} regulating transistors' operation region. In particular, the VCO active core negative resistance is also tuned through the bias current and the gate voltage V_B. However, differently than in [17], the active core is never switched, since changing transistor dimensions does not help improve noise [16]. On the other hand, it can increase circuit complexity or even compromise performance due to the addition of the switches.

2.3.3 Programmable Divider

To support seamless dithering on a wide-range divide modulus we implement a modular PLL divider architecture based on [18]. The divider consists of a cascade of divide-by-2/3 cells (Fig. 2.5) and exploits a hybrid CMOS/CML style to trade speed with phase noise and power consumption. Since M cells provide division ratios from 2^M to $2^{M+1} - 1$ (controlled by inputs P), we need eight cells to cover a 256–511 range. Moreover, by shunting out cell C7 (using an additional control bit P8) we can use the first seven cells to cover ratios between 128 and 255. The four highest frequency cells adopt differential CML whereas the remaining ones leverage full-swing single-ended static-CMOS.

While the above structure is enough for integer division, additional logic is needed for correct fractional-N mode operation. In fact, with a third order modulator, we expect the modulus to vary in the $[N-3N+4]$ interval because of dithering. Therefore, for N in [252–258], smooth swapping between 7-cell and 8-cell configuration is needed with no violations. To support seamless switching, we employ bit P8 to control a multiplexer that mutually selects the divider output F8 (output of cell 8) or F7 (output of cell 7). At the same time, we take care that F8 is always preset to a known value, before its selection, to avoid glitches. Finally, we re-time the divider output via a higher frequency signal (e.g. the output of cell 5) to clear out modulus dependent jitter.

The sigma-delta modulator driving the divider modulus is MASH 1-1-1 with 24-16-8 bit accumulators [19], but can also be configured as a MASH 1-1. A 22-bit linear feedback shift register (LFSR) is included for dither addition to the LSB.

2.4 Receiver

In the following pages, all circuit blocks of the receive chain, from the RF LNA down to the integrated SAR ADC, will be discussed.

2.4.1 Low-Noise Amplifiers

As shown in Fig. 2.6, in the receiver, four parallel LNAs (1–2–3–5 GHz) amplify the wide frequency range (100 MHz–6 GHz) of the input signal with NF down to 1.5 dB. They provide some selectivity against far out-of-band interference and reduce loss

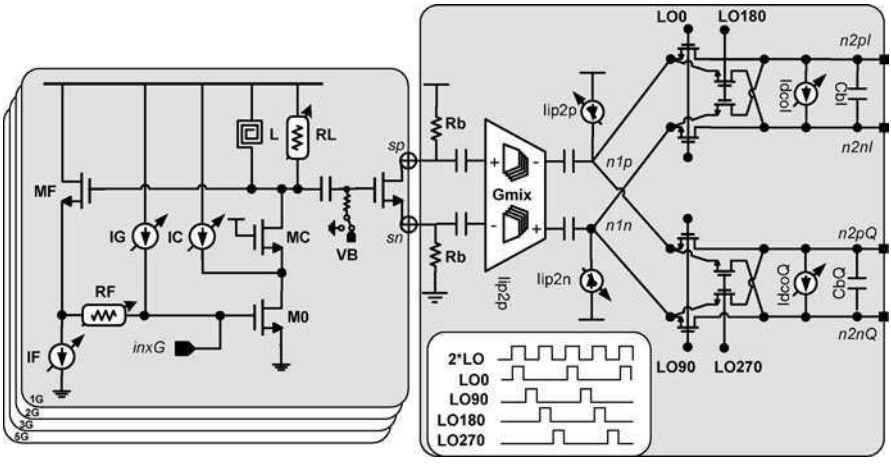

Fig. 2.6 Receiver RF circuit details

and cost of the multi-band antenna interface. Each LNA uses shunt-shunt feedback to provide input matching, and a low-area stacked inductor for gain shunt peaking, keeping the LNA area below 0.02 mm^2 [13]. The input matching condition and the noise factor (F) of the LNA are given by

$$g_{mf} = \frac{1}{R_s.(1+g_{m0}.Z_L) - R_F}, [Z_L = R_L || j\omega L]$$

$$F \approx 1 + \frac{\gamma_0}{g_{m0}.R_s} + \frac{R_F}{R_s(1+A_v)^2}, [A_v = g_{m0}.Z_L] \tag{2.1}$$

where g_{m0} and g_{mf} are the transconductances of the transistors *M0* and *MF* respectively, γ_0 is the (drain current) noise coefficient of the transistor *M0* and R_s is the source resistance to which the input impedance of the LNA should be matched to. As can be seen from the equations, the NF can be lowered by increasing the transconductance of the input transistor at the cost of increased power consumption. This topology offers design freedom in setting NF, gain and input impedance orthogonally. Load (R_L) and feedback resistors (R_F) are made tunable to achieve a minimal gain step of 3 dB, and to find optimum gain setting for achieving certain linearity and NF over different standards. Current bleeding through I_C lowers the voltage drop over the tunable load resistor improving linearity and noise.

Every LNA output is AC coupled and drives one of the four inputs of a multiplexing linear active balun. This is implemented by linear NMOS transistors (M_B) which convert the voltage output of an LNA into a current which flows through R_B creating differential voltage across nodes *sp* and *sn*. At peak gain (and lowest noise) setting, the LNA together with balun consumes a maximum of 20–38 mA from the 1.1 V supply, depending on the desired operating frequency band.

2.4.2 Passive Mixer and IIP2 Calibration

The RF down-conversion to zero-IF is performed by a current-driven double-balanced passive mixer. The passive mixer topology is chosen for its good linearity performance while keeping low 1/f noise and easy operation over a wide RF frequency range.

As shown in Fig. 2.6, at the RF input of the mixer, the received voltage (the output of the balun) is converted into current by an array of binary-scaled transconductors (*Gmix*), based on self-biased CMOS inverters. This array provides supplemental gain control of the receiver's RF front end. It consumes a maximum of 17 mA from the 1.1 V supply.

The resulting current is injected into the two switching quads for in-phase (I) and quadrature-phase (Q) down-conversion. The sources of the NMOS mixer switches are biased at half of the supply voltage by the baseband amplifiers. A 25% duty cycle LO provides 3 dB improvement in the gain of the mixer and hence improvement in the mixer's noise figure compared to the counterpart driven by LO with 50% duty cycle [20].

The 25% duty cycle LO signal is generated from the double-frequency signal coming out of the PLL. A rail-to-rail CMOS dynamic divider is placed closely to the mixer to limit LO-to-RF coupling. An AND-gate uses this to window the original 2LO signal, such that only one out of every two 2LO pulses passes, which results in a clean 25% duty cycle LO signal with minimal phase noise.

Finally, the baseband differential I and Q signals are obtained across the nodes *n2pI, n2nI* and *n2nQ, n2pQ* respectively. The baseband capacitor *CbI/CbQ* gives some initial out-of-band blocker selectivity before the output current is converted into a voltage by means of a trans-impedance amplifier (see Sect. 2.4.3).

As in all direct-conversion receivers, particular care must be paid to the minimization and/or calibration of second-order distortion components. In order to stop the leakage of second order distortion components from the RF blocks, the mixer transconductor is AC-coupled at both the input and the output. RF-to-LO or LO-to-RF coupling are limited by proper isolation and careful layout. The remaining source of second order input interception point (IIP2) degradation is the mismatch between the mixer switches [21]. Since sizing for intrinsic matching is impossible, we propose here a current injection into the positive/negative inputs of the switching quads, in contrast with [20] and [22] where a more conventional gate voltage fine tunability was proposed. The current injection has the advantage that it can be directly applied to an existing mixer core, without the need to split and reroute the LO distribution to the switch gates. Two bidirectional 6b current-steering DACs (*Iip2p* and *Iip2n*) inject small dc currents at nodes *n1p* and *n1n*. This IP2 compensating current will marginally modify the differential bias of the switches, compensating for either threshold voltage and mobility differential mismatches and therefore improving the receiver's second order distortion performance. The injected DC current also flows into the baseband and generates DC offset there, but this is easily corrected by the baseband DC offset compensating DACs *IdcoI* and *IdcoQ*. The IIP2 tuning is implemented directly after the RF transconductor and therefore impacts both quadrature paths. As a consequence, the second order distortion on both quadrature paths cannot be considered independently and therefore the IP2 performance should be evaluated from the complex receiver output, i.e. taking into account the amplitude and phase of the tones at the intermodulation frequency of both quadrature outputs. Analysis and measurements have shown that tuning *Iip2p* and *Iip2n* offers to minimize the complex second order intermodulation distortion measured from the receiver's quadrature outputs with a non-negligible but small impact on the receiver's DC offset. The impact of the compensation currents to suppress the residual DC offset (*IdcoI* and *IdcoQ*) on the overall second order intermodulation distortion is however marginal. Automatic calibration can be performed in the receiver warm-up process or idle-time by generating calibration tones on-chip using the transmit path and exploiting a bilinear search algorithm in the receiver's digital baseband that is able to converge in a few steps, resulting in a complex RX IIP2 performance better than 50 dBm in all operating modes. Once this is fixed, the DC offset can be tuned on-line, together with other calibrations like quadrate accuracy as described in [23].

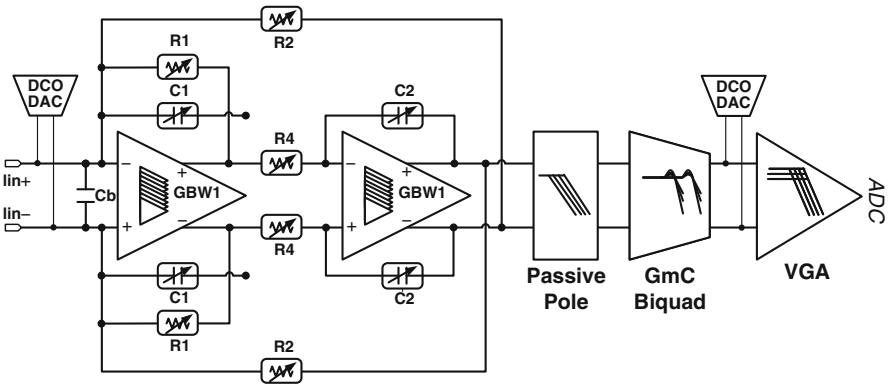

Fig. 2.7 Receiver analog baseband section

2.4.3 Analog Baseband Chain

Based on a Tow-Thomas biquad topology, the transimpedance amplifier (TIA) converts the mixer's current output into a voltage signal by guaranteeing very low input impedance over frequency for improved out-of-band linearity. The TIA input impedance is given by:

$$Z_{in} = \frac{R_1}{(1+sC_1R_1)\cdot[1+A_1(s)]\cdot[1+LG(s)]} \tag{2.2}$$

where R_1 and C_1 are shown in Fig. 2.7, $A_1(s)$ is the open loop gain of the first amplifier, with gain-bandwidth product GBW_1, and $LG(s)$ is the open loop gain of the Tow-Thomas biquad derived as:

$$LG(s) = -\frac{R_1}{sR_2R_4C_2\cdot(1+sC_1R_1)} \tag{2.3}$$

Z_{in} is very close to zero at low frequencies, while it may increase at high frequencies, depending on the GBW of the first opamp. A maximum simulated out-of-band third order input interception point (IIP3) of 14 dBm can be achieved with a GBW of 400 MHz. To further reduce the out-of-band Z_{in} and boost out-of-band linearity, a capacitor C_b is placed across the virtual ground nodes.

Two complex conjugated poles (hence a 40 dB/decade attenuation) are generated with pole frequency ω_p and quality factor Q given by:

$$\omega_p = \frac{1}{\sqrt{R_1R_4C_1C_2}} \qquad Q = \frac{R_1}{\sqrt{R_2R_4}\cdot\sqrt{\frac{C_1}{C_2}}} \tag{2.4}$$

To achieve flexible frequency discrimination and gain control, we employed binary-scaled arrays of analog components connected in parallel, as in [24]. Special care was placed in reducing silicon area and in sizing the array switches carrying useful signals. The switches are implemented as NMOS-PMOS transmission gates, and connected, whenever possible, to low impedance nodes.

Differently than in a simple integrator, biquad parameters in our topology can be independently tuned. For instance, R_1 can be adjusted to achieve the specified Q, as suggested by (4), without changing the cut-off frequency; R_2 and R_4 can be tuned to configure the trans-resistance gain (from 1 to 8 kΩ) while keeping the bandwidth constant. By using this approach, Q can be tuned from 0.53 to 1.5, the cut-off frequency covers the range between 0.5 MHz and 20 MHz (or higher). Moreover, the switchable opamps approach [24] helps trade power consumption for bandwidth whenever lower out-of-band blockers are detected or lower cut-off frequencies are required.

After the TIA, many standards require further attenuation as the interferer power might be still quite high. As an active filtering block at this point would still need high out-of-band linearity, we decided to further attenuate interferers by using a flexible passive pole. Consequently, the final filter stage is a cheap Gm-C inverter-based biquad, as in [25], whose noise/linearity performance is not critical. Together with the TIA poles, the overall baseband provides flexible fifth order selectivity, but it can be conveniently switched to a third order if the Gm-C filter is bypassed. A VGA further maximizes the dynamic range with 24 dB gain in 16 logarithmic gain steps. As shown in Fig. 2.7, the DC offset is compensated at the virtual ground of the TIA and the VGA by injecting current in discrete steps through 6-bit current steering DACs.

2.4.4 SAR ADC

The ADC used in the receiver is based on the low-power charge-sharing SAR ADC architecture proposed in [26, 27]. This architecture offers sufficient speed for the intended applications, and lends itself very easily to integration in a nanoscale CMOS process, as the only active element is a comparator combined with capacitors, switches and a digital controller.

The ADC block diagram is shown in Fig. 2.8. It includes a time-interleaved bootstrapped S/H, a passive charge-sharing DAC, a redundant comparator topology and an asynchronous controller. As capacitor matching performance improves with technology, the resolution of the original 9 bit design in 90 nm [26, 27] could easily be extended to 10 bits without the need to increase the total capacitance value by a factor 4. The unit cap is chosen to be 30 fF. The least significant bits are constructed not by binary scaling the capacitance value but by pre-charging them to a lower voltage as in [26]. The flexible comparator scheme as in [27] uses a high-noise (HN) comparator in the first nine decisions and a low-noise (LN) comparator in the last one, and an extra decision for redundancy check to achieve almost 1-ENOB

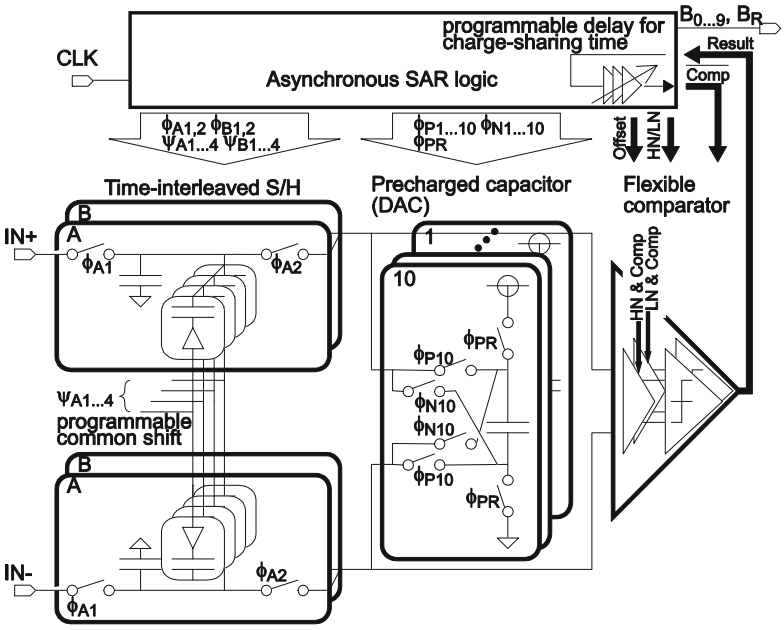

Fig. 2.8 10 bit SAR ADC block diagram

improvement with low extra power. The comparator itself is based on [28]. It uses a dynamic pre-amp for low noise, and achieves an excellent noise/power trade-off.

The common-mode level (CM) at the comparator's inputs involves two important trade-offs. The settling speed of the charge-sharing is mainly determined by the NMOS sharing switches on-conductance, which is limited by the rather high threshold voltage combined with the low supply voltage of this low-power 40 nm process. To boost the conversion speed, the CM must be kept as low as possible. Hereto, the CM is shifted down right after the sampling operation. This has however also a significant impact on the thermal noise of the comparator and hence on the overall effective ADC resolution. This is even more important considering the increase of noise excess factor (γ) in our 40 nm process and the strong dependence of the comparator pre-amplifier gain on the overdrive voltage of input-stage. As a compromise between noise and speed, a CM voltage around 0.33 V was chosen.

The total ADC achieves >9 effective bits resolution at a power budget of less than 1 mW, which is negligible in the total power budget. This is exploited in the receiver system budget by keeping the sampling frequency rather high, even for low-bandwidth standards. This oversampling allows to reduce the channel select filter's order, as there is no need to suppress interferers that would otherwise be aliased down to baseband by the sampling [4].

2.5 Transmitter

The SDR transmitter must support multiple standards at various transmit frequencies. These standards include FDD standards, in which the transmitter is active while receiving. The transmitter emits, besides the wanted output signal, unwanted out-of-band noise as well. This noise is then further amplified by the external power amplifier before being fed to the duplexer, which connects the receive/transmit input/output with the antenna (Fig. 2.9). As the isolation between RX and TX is not infinite, part of the transmit out-of-band noise ends up at the input of the receiver and adds effectively to the receiver system noise. Traditionally, this transmitter noise is filtered by adding an interstage surface acoustic wave (SAW) filter between the integrated pre-power amplifier and the external power amplifier. As this adds up to the system BoM cost and reduces the flexibility, it is commercially attractive to avoid this interstage filter, which puts very though requirements on the out-of-band noise specifications of the transmitter.

The carrier-to-noise ratio (CNR) specifications for SAW-less FDD transmitters should be defined considering the complete system, including both receiver and transmitter and the external components. Figure 2.9 shows one example scenario. A receiver with a NF of 3.5 dB is considered and from system analysis, a maximal degradation up to a NF of 4.2 dB is acceptable. The transmitter noise power density which is acceptable at the receiver input for this condition is $-178\,\mathrm{dBm/Hz}$. For a duplexer isolation of 50 dB, the out-of-band noise at the output of the power amplifier is maximally $-128\,\mathrm{dBm/Hz}$. For a PA with a gain of 27 dB, the maximal noise at the output of the integrated pre-power amplifier is $-155\,\mathrm{dBm/Hz}$ if the interstage SAW filter is omitted. For an output power of $+24\,\mathrm{dBm}$ at the antenna, and an insertion loss of 3 dB in the duplexer, the RMS power at the output of the PPA is 0 dBm, and the required CNR is thus $-155\,\mathrm{dBc/Hz}$. From this analysis it is clear that the final CNR requirement for the transmitter has a certain variability that depends on external and system considerations, such as the isolation of the duplexer and the NF of the receiver and the degradation we can afford.

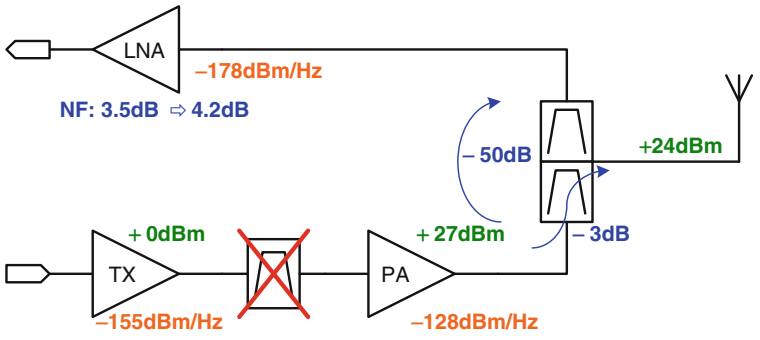

Fig. 2.9 SAW-less transmitter operation in FDD mode

Transmitter out-of-band noise has a significant contribution from upconverted baseband noise. To limit this contribution, the out-of-band noise at baseband has to be intrinsically low or filtered out before being upconverted. In a traditional current mode Gilbert active mixer, the baseband signal is a current and its noise component, which also includes the noise of the mixer's bias current, is very hard, if not impossible to be filtered, as it is a current as well. As the current-mode noise cannot be filtered at baseband and as we do not want to filter it with a SAW filter at RF, a current-mode upconverter requires an intrinsically low noise mixer design. This results however in a large power consumption, in the order of what is typically needed in a pre-power amplifier. As a result, in a current-mode design the mixer has to be combined with the PPA into a power mixer to maintain power efficiency [29].

If a voltage based design is considered, the baseband noise can be filtered easily in the voltage domain, which results in less stringent intrinsic noise requirements for the baseband, and in lower power consumption. For this reason, a voltage sampling mixer [14] was chosen for the presented SDR transmitter. The mixer is followed by a pre-power amplifier (PPA), whose noise contribution should be sufficiently low as it cannot be filtered at RF. This results in a non negligible current consumption, and as a result only a single stage is affordable in the PPA, as adding an extra stage would result in high power consumption.

Besides out-of-band noise, power control is another important aspect in the transmitter. The strategy adopted in the presented transmitter is to distribute the coarse gain control over the three main building blocks, while reserving one baseband DAC bit (6 dB) for digital fine tuning of the gain. From output to input, the PPA has a gain tuning range of 36 dB, the Mixer of 12 dB and the TI-LPF of 18 dB. By adding the 6 dB fine tune digital gain, a total control range of 72 dB is implemented.

The total transmit chain architecture is depicted in Fig. 2.10, whose individual blocks are described in more detail in the next sections.

2.5.1 The Transmit Baseband Section

The transmitter's baseband section is actually a copy of part of the receiver's channel select filter, where again the reconfigurability of the SDR philosophy is used that allows achieving the desired performance by simply reprogramming it into the corresponding mode. It consists of a Tow-Thomas transimpedance biquadratic low-pass section (TI-LPF) with programmable bandwidth (400 kHz up to more than 20 MHz) and a passive pole to filter out out-of-band noise.

Similarly to the receive baseband, scalable opamps are used of which the gain-bandwidth product can be adjusted in eight steps from 60 to 480 MHz, exchanging filter's linearity for current consumption [24]. The DC offset can be compensated by injecting a small DC current at the input of the TI-LPF through integrated calibration current DACs.

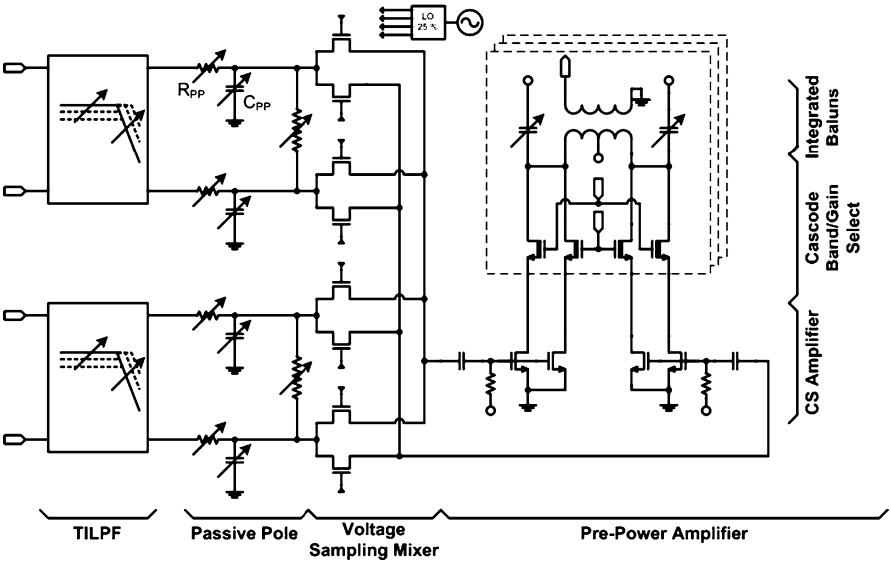

Fig. 2.10 TX block diagram

2.5.2 The Mixer

The mixer is the heart of the transmitter and the key component for low-noise operation. As discussed above a voltage-mode mixer was chosen, as it offers the possibility of baseband noise filtering before the upconversion. In this design, we adopt a differential direct voltage sampling mixer [14]. The baseband signals from the TI-LPF are first filtered by a passive RC low-pass filter (Fig. 2.10). This reduces the required noise performance of the preceding stage, which limits its power consumption. The baseband voltage is sampled alternatively from I and Q with a 25% duty cycle LO signal onto the load capacitance, which is actually the input capacitance of the subsequent PPA. The sampling behavior of the mixer results in charge and discharge currents from the baseband section that must flow through the passive pole's resistor. The resulting voltage drop reduces the overall mixer's conversion gain. As the charge currents are proportional to the LO frequency and the load capacitance, and the voltage drop over the LPF is proportional to its resistive component, the effective mixer's conversion gain (CG) is given by [30]:

$$CG = \frac{2\sqrt{2}}{\pi} \times \frac{Z_{mix}}{R_{PP} + Z_{mix}}$$

$$Z_{mix} = R_{sw,on} + \frac{1}{2 \cdot F_{LO} \cdot C_{load}} \tag{2.5}$$

where R_{PP} is the value of the passive pole resistor, Z_{mix} is the mixer input impedance, $R_{sw,on}$ is the on-resistance of the LO switches and C_{load} is the input capacitance of the load, i.e. the PPA.

The mixer must therefore be carefully co-designed with the active LPF impedance and with the PPA load, considering the full system requirements, as the LO frequency and the input capacitance have an impact on the mixer's conversion gain when combined with the passive pole's resistor. The latter has an impact on the linearity and noise requirements of the active LPF and on the area (a small resistor requires more driving strength of the TI-LPF, and a bigger passive pole's capacitor for a given filtering). In our design, a nominal value of 300Ω was chosen as a compromise between noise filtering and gain roll-off at higher frequencies. Note that the resistor of the passive pole is tunable. In combination with a second tunable resistor, 12 dB of gain variability is obtained in the mixer.

As the voltage sampling mixer core is fully passive, the only contributor to the power consumption is the 25% duty cycle generator. Its design is based on CMOS-like rail-to-rail logic, with proper sizing to achieve sufficient low phase noise.

2.5.3 The Pre-power Amplifier

The final stage in the transmitter is the pre-power amplifier (PPA). It takes the upconverted signal from the mixer, amplifies it and feeds it to the 50Ω input of an (off-chip) power amplifier. The PPA has to combine low noise for FDD operation with high linearity for EVM and ACPR performance. From a cascade analysis, the PPA has to achieve 10 dB differential to single-ended voltage gain. As discussed before, this gain has to be realized in a single stage to limit the current consumption. Furthermore, as the PPA's input capacitance is the sampling capacitor of the mixer, the PPA size is limited to avoid excessive mixer conversion gain degradation.

The PPA schematic is modular and is presented in Fig. 2.10. It consists of a set of parallel Common Source (CS) amplifiers, which can be turned on or off by thick oxide cascode transistors. The latter protect the 40 nm CS transistors from the 2.5 V supply, provide discrete 6 dB gain control steps and select one out of three possible outputs. As part of the PPA is turned off when gain and output power are reduced, the DC power consumption is proportional to the output power. This is especially beneficial, as in most practical situation (e.g. as described in DG09 [31]), operation at maximal output power is limited in time.

The PPA has been implemented pseudo differentially and fits with the differential mixer. Three on-chip baluns have been integrated to provide single ended outputs. The baluns consist of a transformer realized in the two top metal layers of the technology that are approximately 0.8 µm thick. Their primary windings include a center tap to provide the DC bias current of the amplifier. The transformers were designed by combining two ASITIC [32] generated coils. This simulator was also used to derive a simplified transformer model, including the limited coupling, the limited Q-factor and the parasitics to ground and between both coils. This approach

using a simplified model speeds up the exploration phase of the design. When the final balun dimensions were defined, the simplified model was validated with a more precise finite-element generated model. Although the PPA core is intrinsically wide-band, the baluns introduce some bandwidth limitation. The center frequencies of the baluns are defined with a tunable parallel capacitor and spread over the frequencies from 700 MHz up to 3 GHz. In this prototype, the center frequency balun has been bypassed to provide a wide-band differential output for testing purposes. This can be combined with an external balun or differential amplifier as required. Measurements have been successfully performed both with internal and external baluns.

2.6 Measurement Results

The microphotograph of the complete SDR prototype with the most important blocks annotated is shown in Fig. 2.11. It is implemented in a 1.1 V 40 nm LP CMOS technology and measures 2.0 by 2.5 mm^2.

After an initial design in 45 nm technology that was slightly off-centered [15], the tuning range of the new dual VCO set in 40 nm CMOS covers the full range from 5.95 until 12.85 GHz as shown in Fig. 2.12. The VCO gain is calibrated to be

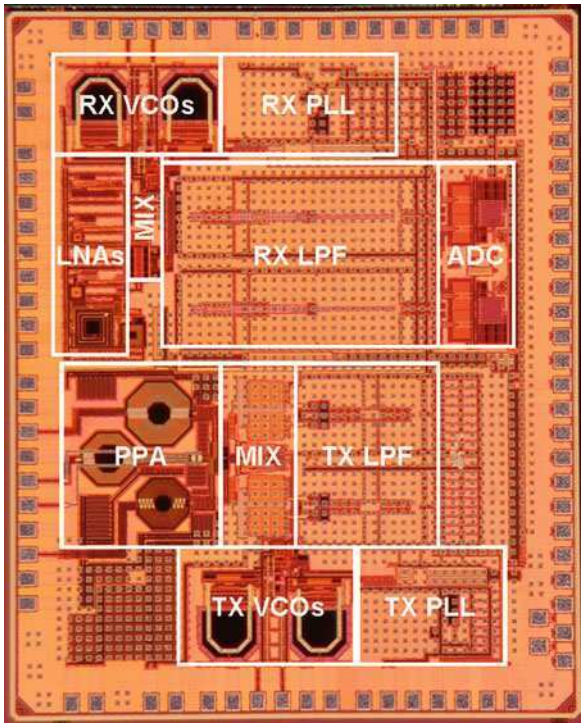

Fig. 2.11 Microphotograph of the complete transceiver

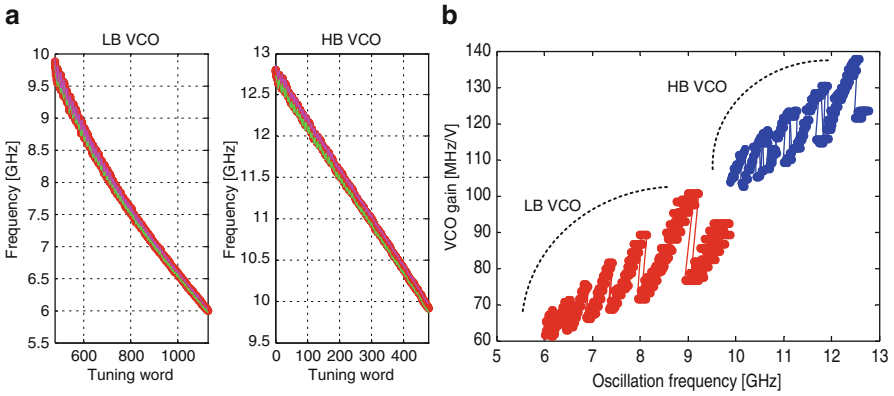

Fig. 2.12 (**a**) Total frequency range spanned by the two VCOs; (**b**) VCO gain programmed to be proportional to the center frequency

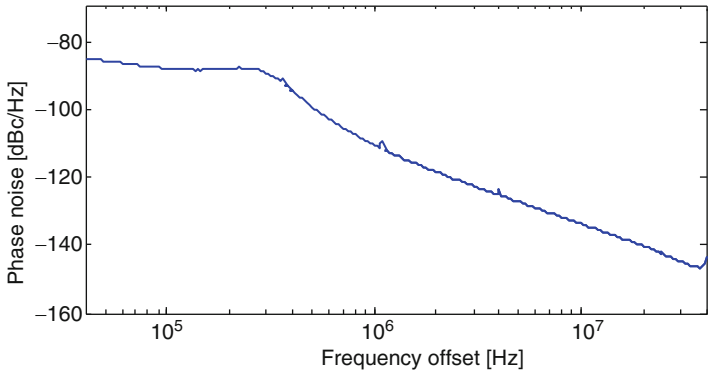

Fig. 2.13 PLL phase noise measurement at 7.2 GHz

proportional to the center frequency, using a procedure adapted from [17], as this results in a constant PLL BW for a fixed charge pump and loop filter.

The closed-loop PLL phase noise at 7.2 GHz shown in Fig. 2.13 yields −32 dBc in-band integrated phase noise. The measured phase noise value at 20 MHz offset frequency is −140 dBc/Hz, which could be extrapolated to −158 dBc/Hz at 900 MHz operation after division be 8. The 40 MHz reference spur sits at −80 dBc. The full synthesizer draws 30–40 mA from the 1.1 V supply

To evaluate the receiver's RF performance, it is measured at baseband at the output of the TI-LPF (which converts the mixer's output current to voltage). The input matching of the different LNAs is shown in Fig. 2.14a. In the frequency of interest, each of the LNAs provides S11 better than −10 dB. The measured maximal gain of the receiver (LNA, mixer and TI-LPF) is approximately 75 dB (with a peak of 77 dB) and gradually decreases at high frequency (around 5 GHz and

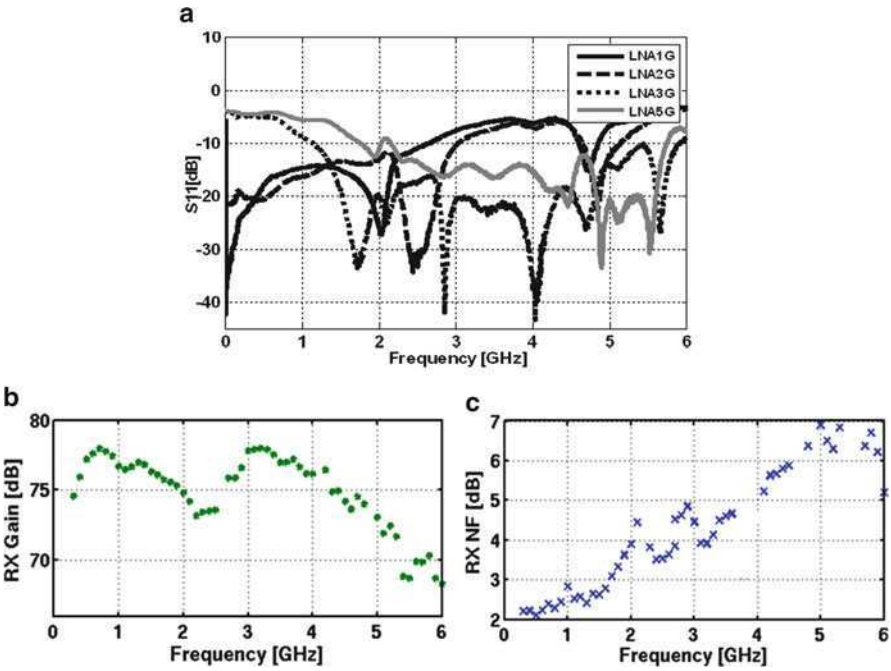

Fig. 2.14 Measured RX RF performance; (**a**) input matching; (**b**) gain; (**c**) noise figure

beyond) below 72 dB due to the combined effect of LNA and mixer's gain roll-off. The peaks and dips over the frequency range are due to fact that the gains of the various LNAs are not exactly matched and different LNAs are chosen to operate at different frequencies. The measured NF of the receiver at peak-gain settings is shown in Fig. 2.14c. The total NF ranges from 2.3 dB to 7 dB over the frequency range. The peaks and dips in the NF plot are due to the dependency of NF on RX gain.

Figure 2.15a shows the measured IIP2 performance for the whole tuning range of both 6 bit IIP2 DACs on each differential line. The receiver operates at 5 GHz with a channel bandwidth of 20 MHz and at maximal gain. Two out-of-band CW blockers at arbitrary offset frequencies of 83 and 85 MHz are provided to the receiver input. The default IIP2 performance of 41 dBm (configuration 0/0 in Fig. 2.15a) can be improved in the measured area up to 65 dBm (configuration 23/1). Extensive measurements over different modes show a consistent improved IIP2 performance beyond 60 dBm, which is enough to cope with the toughest FDD cellular requirements. Figure 2.15b shows the (negligible) impact of IIP2 calibration on NF performance.

The RX analog baseband can be separately tested thanks to on-chip test circuitry that allows providing an external input signal to the TIA input. From a 2-port network analyzer measurement, the several transfer function settings are shown in Fig. 2.16a for 0 dB voltage gain. The low-pass filter's bandwidth ranges from

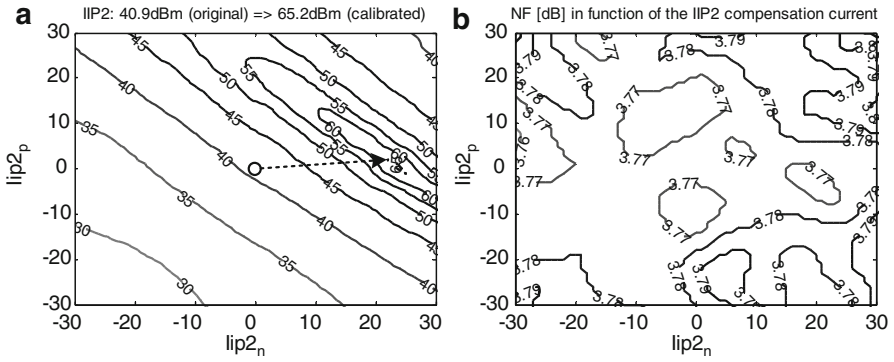

Fig. 2.15 (**a**) Measured IIP2 performance over the IP2 control tuning range; (**b**) impact of IP2 tuning on the receiver system NF

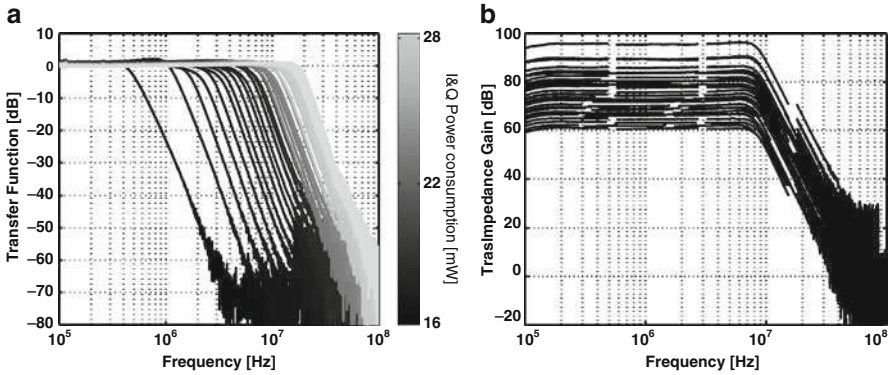

Fig. 2.16 (**a**) Analog baseband transfer function, including VGA, for a constant 100 dB/dec selectivity and different bandwidth/power consumption levels; (**b**) possible AGC settings for the analog baseband section

0.5 up to more than 20 MHz, while the transition bandwidth is kept constant and allows up to 100 dB/dec Butterworth-like attenuation. Power consumption scales with the bandwidth from 16 to 28 mW: these numbers include TIA (50%), Gm-C filter (10%) and VGA (40%), for both I and Q channels. In addition to this coarse tuning capability, the cut-off frequency can be tuned with a maximum 5% error to compensate for ±40% process deviation. Figure 2.16b shows all the possible transimpedance gain settings of the analog baseband; the gain range is about 36 dB while the minimum gain step is below 1 dB. The influence of baseband DC offset is negligible in both these tests.

The ADC is measured separately, as reported in Fig. 2.17. The maximal sampling speed is 60 MS/s, with a power consumption of 1.2 mW. At lower speeds, the power decreases proportionally. An SNDR of 54 dB (9.3 ENOB) is obtained. Maximum DNL and INL are ±1.4 and ±0.8 LSB, respectively. Using the classical figure-

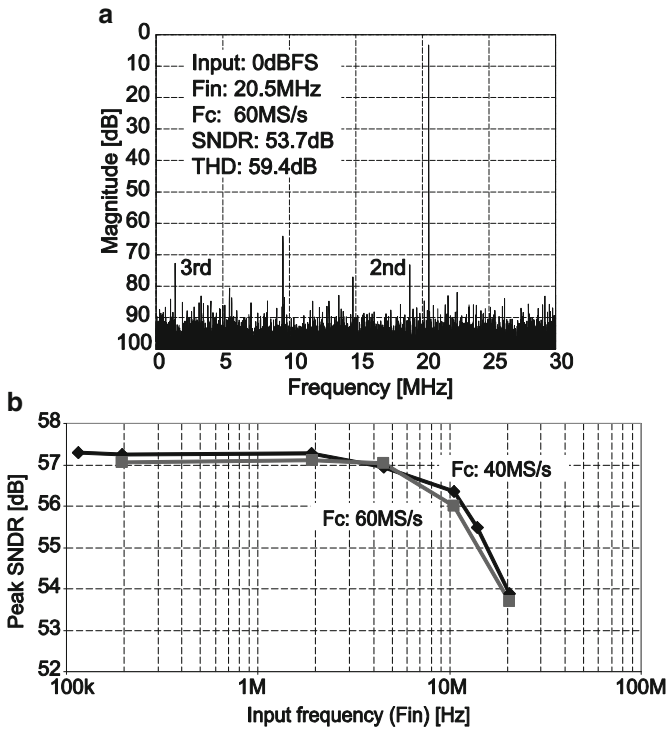

Fig. 2.17 Measured ADC performance: (**a**) near-Nyquist FFT; (**b**) SNDR vs input frequency

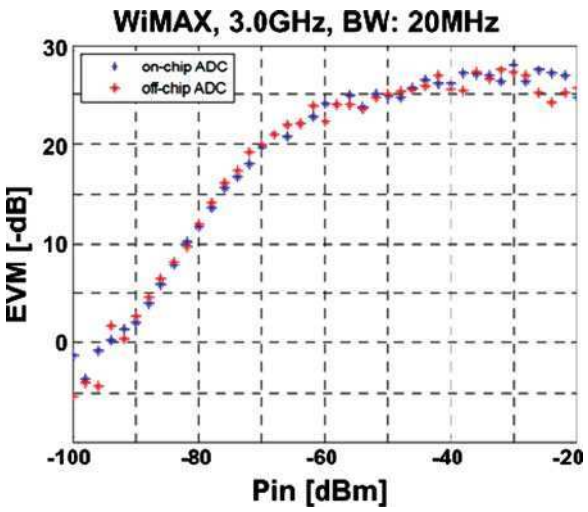

Fig. 2.18 Measured RX EVM performance with and without on-chip ADC

Table 2.1 RX + LO performance summary and comparison with CMOS state-of-the-art

Mode	Ref	CMOS node	Area (mm^2)	NF (dB)	IIP3 (dBm)	IIP2 (dBm)	PDC (mW)
DVB-H	This work	40 nm	5	2.6	−4.6/+9	53	55–83
0.2–0.7 GHz	[33]	65 nm	7	2.2	−6/−3	40	138
GSM/EDGE	This work	40 nm	5	2.4	−17/−4.7	64	54–77
0.9 GHz	[34]	90 nm	7.4	2	−25/−20	46	84
WCDMA	This work	40 nm	5	2.4/4	−9/−6	68	55–84
0.85/2.1 GHz	[35]	130 nm	8.7	2.5/3	−5	55	48
GPS	This work	40 nm	5	2.6	−3/−4	56	54–77
1.5 GHz	[36]	130 nm	6.6	2.5/3	25/−23	43	49
MIMO WiMAX	This work	40 nm	10	3.8	−12/−1	61	112–214
2.5 GHz	[37]	90 nm	12	3.5	−11/12	N/A	300
MIMO WLAN	This work	40 nm	10	3.4/7	−15/−8	59	112–270
2.4/4.8 GHz	[38]	180 nm	18	4/4.5	−12/6	N/A	495

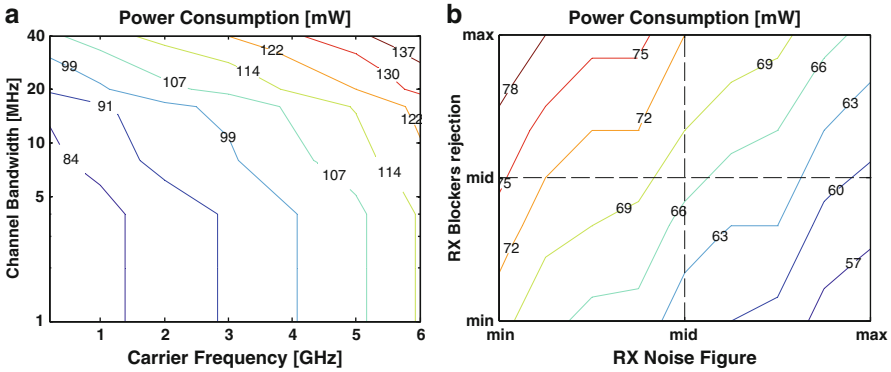

Fig. 2.19 RX + LO Energy awareness: (**a**) Measured Receiver Power Consumption over all the RF frequency range and channel bandwidth. (**b**) Possible range of power consumption in GSM receiving mode by the required noise/selectivity and linearity requirements

of-merit formula, $FoM = P_{DC}/(2^{ENOB}.F_S)$, a value of 34 fJ per conversion step is obtained. Figure 2.18 reports the measured RX EVM performance in 3 GHz WiMAX mode (20 MHz BW), either using the analog output of the VGA or with the on-chip ADC, showing no significant difference

Table 2.1 compares the performance measured on the presented RX + LO circuits with state-of-the-art CMOS transceivers under different configuration modes showing in most cases comparable performance, area and power consumption. One of the unique features of an SDR transceiver is its energy awareness: Fig. 2.19a shows how the RX + LO measured power consumption changes according to the required

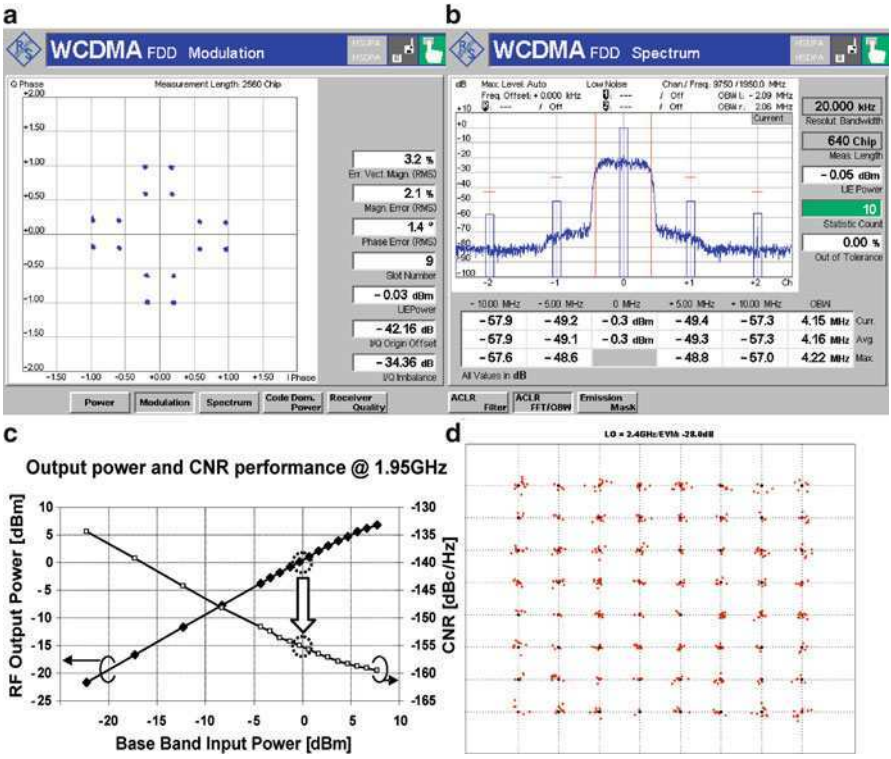

Fig. 2.20 TX performance: (**a**) WCDMA constellation diagram; (**b**) output spectrum; (**c**) output power and noise at 1.95 GHz; (**d**) EVM for 802.11 g 64QAM at 0 dbm output power

operational mode. While a GSM operation at 900 MHz and small bandwidth will require a maximal power consumption of about 80 mW, a Wi-Fi .11n at 5 GHz and 40 MHz channel bandwidth will require about 130 mW. On top of such standard-related trade-offs, it is also possible to provide run-time energy awareness by sensing the environmental conditions. Blockers could for example be sensed by adding power detectors at various filtering stages in the receive chain, SNR could for example be sensed to tune the receiver to a 'minimal margin' scenario. To exemplify this, Fig. 2.19b shows how a GSM mode power consumption can actually change based on the required noise/linearity performance of the receiver and an AGC algorithm that guarantees just a good-enough SNR rather than maximal SNR. Receiving a call in the centre of the city will not require 2 dB RX noise figure (NF). Or receiving in the countryside is likely not to impose the toughest blocking conditions foreseen by the standards. Such trade-offs will allow to save energy where/when possible.

To measure the transmitter, the I/Q baseband signals are converted from the voltage of the measurement equipment into a current needed for the TI-LPF reconstruction filter input over an external 5 kΩ resistor. The main transmitter

measurements are presented in Fig. 2.20 in for various modes of operation. An output 1 dB gain-conpression point (OP1dB) of around 7 dBm has been measured with the integrated baluns from 850 MHz up to 2 GHz and better than 4 dBm up to 2.5 GHz. A linear OFDM and WCDMA modulated signal with an EVM from 2.7 to 4% was measured up to 0 dBm output power. At 2.5 GHz, 2.5% EVM was achieved with an external LO for −2.5 dBm output power. An 8-PSK modulated signal up to 4.8 dBm was measured at 850 MHz with a spectral mask better than −61 dBc at 400 kHz offset. At 1.8 GHz, 1 dBm output power was measured.

The CNR was measured in two ways. First, a single tone was transmitted by applying a DC signal at baseband, and a phase-noise analyzer was used to determine the noise floor of the transmitter. This was then subtracted from the maximal linear RMS output power (that needs a certain back-off from OP1dB, depending on the modulation) to obtain the CNR. For the EDGE-mode of operation, a CNR of −156 dBc was measured at 20 MHz offset for a 900 MHz carrier with an external LO. The main noise contributor in this mode is baseband noise from the active filter, which is not filtered by the passive pole, due to its relatively high cut-off frequency. For WCDMA mode, a full linear WCDMA signal was transmitted. The TX band signal was filtered by a reversed duplexer (transmitter at output port), and the noise at the RX port in the receive band was measured, after de-embedding of the duplexer's insertion loss. These measurements result in −156 dBc/Hz at 45 MHz offset for an 850 MHz LO and −153 dBc/Hz at 190 MHz offset for a 1,950 MHz LO. When using an external LO, −156 dBc/Hz was obtained for the 1,950 MHz case as well. At 1.95 GHz, the transmitter's CNR is mainly limited due to the phase-noise generated in the LO 25% duty cycle generator. It is caused by the jitter introduced by the limited relative speed of the LO signal's edges. When using the internal VCO, its phase noise and the noise of the first LO buffer at 7.8 GHz is added to this. At 850 MHz, the limitation comes from the baseband noise due to the smaller (45 MHz) offset between TX and RX band and the resulting reduced filtering from the passive pole and the active second order filter.

The power consumption of the transmitter varies with the required performance. Depending on the output power (TRA linearity/PPA Gain) and the frequency (LO25), the transmitter consumes from 20 up to 38 mA from the 1.1 V supply and 6–30 mA from the 2.5 V supply.

Table 2.2 summarizes the main TX measurement results and compares the performance achieved by this TX work with state-of-the-art WCDMA CMOS transmitters.

2.7 Conclusions

In this chapter, we have presented a full transceiver front-end for an SDR platform in a 40 nm LP CMOS process. Quadrature frequency synthesis is obtained with a set of two VCOs covering the 6–12 GHz range embedded in a fractional-N PLL, followed by a chain of rail-to-rail CMOS divide-by-2 circuits. Four parallel LNAs, a 25% duty

Table 2.2 TX performance summary and comparison with CMOS state-of-the-art

RF Freq TX mode	Pout (dBm)	EVM (%)	ACLR1/2 Spectrum (dBc)	CNR (dBc/Hz)	OP1dB (dBm)	LOFT[b] @0dBm (dBm)	IRR @0dBm (dBm)
850 MHz WCDMA Band V	−0.3	2.7	−47/−58	−156@45 MHz	6.7	−66	45
900 MHz EDGE Mode[a]	4.8		Spectrum: −61dBc@400 kHz −74dBc@600 kHz	−156@20 MHz −153@10 MHz	6.7		
1.8 GHz EDGE Mode[a]	1		Spectrum: −65dBc@400 kHz −70dBc@600 kHz	−152@20 MHz −150@10 MHz	7.5		
1.95 GHz WCDMA Band I	0	3.2	−49/−57	−153/−156[a]@190 MHz	7.5	−58	48
2.4 GHz (64QAM/20 MHz) on-chip balun WLAN Mode	−0.5	4.2	−47/−60		4.2	−59	45
2.4 GHz (64QAM/20 MHz) ext. Balun WLAN Mode	0	4	−46/−62		4.7	−59	46
2.5 GHz (64QAM/20 MHz) int Balun/ext VCO WiMAX mode[a]	−2.5	2.5	−46/−62		4.6	−53	43

	CMOS node	Area (mm^2)	ACLR (dB)	@Pout (dBm)	CNR (dBc/Hz)	P_{DC} (mW)	@Pout (dBm)
[39]/[40]	180 nm	5	−42.6	+5	160–3[c]	120	+5
						90	−8
[29]/[41]	180 nm	4.5[c]	−46	+3.8	163	236	3.8
						75	min
[42]	130	7.5[c]	−43	7	161	100	avg
This work	40 nm	1.3	−49	0	156	90	+1

[a]External VCO
[b]LO feed through
[c]Estimated

cycle passive mixer, a fifth order baseband section and an integrated 10 bit 60 MS/s ADC have shown state-of-the art performance for all relevant communication standard scenarios up to 6 GHz. A low-noise transmitter with a voltage-sampling mixer and on-chip baluns is used for SAW-less FDD operation. This prototype once again shows that SDR platforms in nanoscale CMOS technologies are the preferred implementation choice for future ubiquitous mobile terminals.

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Chapter 3
Digital RF and Digitally-Assisted RF

Robert Bogdan Staszewski

3.1 Introduction

3.1.1 Analog-Intensive RF Transceivers

Until around mid-1990s, virtually all radio frequency (RF) transmitters/receivers (transceivers) have been analog intensive and based on an architecture similar to that shown in Fig. 3.1a [1]. On the receiver (RX) path, the signal from an antenna is filtered by a typically-external bandpass filter (BPF) to attenuate out-of-band blockers. The signal is then amplified by a low-noise amplifier (LNA) and downconverted (i.e., frequency translated) to a baseband frequency (dc or a low intermediate frequency, IF, being a fraction of a channel separation) through an image-reject downconversion mixer operating in in-phase ($I \equiv \Re(S)$) and quadrature ($I \equiv \Im(S)$) complex-number signal S domain. $\Re(S)$ and $\Im(S)$ are the real and imaginary components, respectively, of a complex signal S. The signal is then further low-pass filtered (LPF) and amplified before being finally converted into digital discrete-time samples through analog-to-digital converter (ADC or A/D). The digital baseband processes the signal samples to estimate the original transmitted symbols, from which the user information data is obtained.

On the transmitter (TX) path, the user information data gets converted into symbols, which are then pulse-shaped to obtain baseband I and Q digital samples that are frequency-band-constrained. They are then converted into analog continuous-time domain through a digital-to-analog converter (DAC or D/A) with a typical zero-order-hold function. The LPF following the DAC then filters out the switching harmonics. Thus obtained analog baseband signal gets then upconverted (frequency translated) into RF through an image-reject single-sideband (SSB) modulator.

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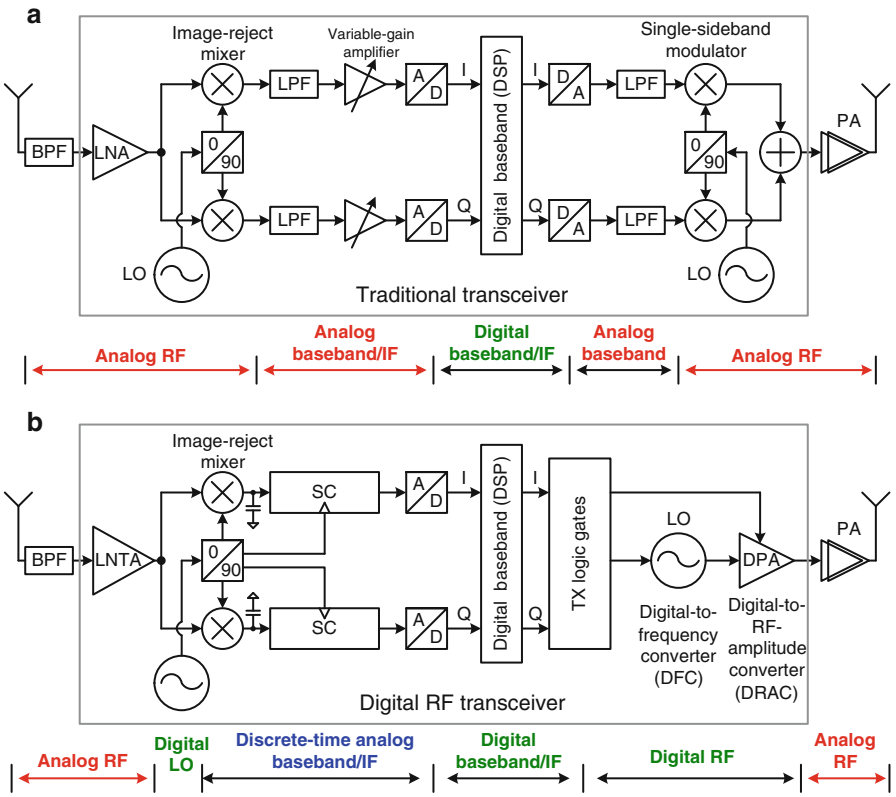

Fig. 3.1 Comparison between (**a**) traditional analog-intensive RF transceiver and; (**b**) new transceiver based on the Digital RF principles

The following (typically external) power amplifier (PA) increases the RF power level at the antenna to that required by the wireless standard, which could be as high as 2 W for a GSM handset. While the complex-number representation of the baseband signal is known to be always I/Q for the receiver, the complex number representation for the transmitter could be realized as either I/Q (shown in Fig. 3.1a) or polar, in which the two orthogonal components are amplitude $A = |S|$ and phase $\phi = \angle S$, or $S = Ae^{j\phi}$. (An example of a TX digital polar modulator is shown in Fig. 3.6 in Sect. 3.4.) The phase modulation could be performed by a direct or indirect frequency modulation of a phase-locked loop (PLL). The amplitude modulation could be performed by V_{DD} modulation of a high-efficiency class-E PA.

The frequency synthesizer-based local oscillator (LO) performs the frequency translation for both the RX and TX. It is typically realized as a charge-pump PLL [2] with $\Sigma\Delta$ dithering of the modulus divider to realize the fractional-N frequency division ratio.

The complete architecture and monolithic circuit design techniques of the conventional transceivers of Fig. 3.1a have been well described in numerous literature and text books, in particular [3,4] and their later editions. The architecture has been successfully used in integrated CMOS transceivers [5] for over a decade (since late 1990s). Unfortunately, its useful lifetime is slowly coming to an end [6] in favor of more digitally-intensive architectures, such as the one shown in Fig. 3.1b.

3.1.2 Digitally-Intensive RF Transceivers

The main reasons behind this sea-like transformation are the ever-improving cost advantages and processing capabilities of the CMOS technology, which have been happening at regular intervals with the pace according to the so-called Moore's Law. Basically, with every CMOS process technology advancement node (i.e., from 130-nm to 90-nm, then to 65-nm, and then to 40-nm, and so on) happening every 18–24 months, the digital gate density, being a measure of the digital processing capability, doubles (i.e., gate area scaling factor of 0.5x). At the same time, the basic gate delay, being a measure of the digital processing speed, improves linearly (i.e., gate delay scaling factor of 0.7x). Likewise, the cost of fabricated silicon per unit area remains roughly the same at its high-volume production maturity stage. Indeed, over the last decade, the cost of silicon charged by integrated circuit (IC) fabs has remained constant at around US$ 0.10–0.25/mm^2, depending on the wafer volume and targeted gross profit margin (GPM). The main implication of this is that a cost of a given digital function, such as a GSM detector or an MP3 decoder, can be cut in half every 18–24 months when transitioned to a newer CMOS technology. At the same time, the circuits consume proportionately less power and are faster.

Unfortunately, these wonderful benefits of the digital scaling are not shared by the traditional RF circuits. What's more, the strict application of the Fig. 3.1a architecture to the advanced CMOS process node might actually result in a larger silicon area, poorer RF performance and higher consumed power. The constant scaling of the CMOS technology has had an unfortunate effect on the linear capabilities of analog transistors. To maintain reliability of scaled-down MOS devices, the V_{DD} supply voltage keeps on going down, while the threshold voltage V_t remains roughly constant (to maintain the leakage current). This has a negative effect on the available voltage margin when the transistors are intended to operate as current sources. What's more, the implant pockets added for the benefit of digital operation, have drastically degraded the MOS channel dynamic resistance r_{ds}, thus severely reducing the quality of MOS current sources and the maximum available voltage self-gain $g_m \cdot r_{ds}$ (g_m is the transconductance gain of a transistor). Furthermore, due to the thin gate dielectric becoming ever thinner, large high-density capacitors realized as MOS switches are becoming unacceptably leaky. This prevents an efficient implementation of low-frequency baseband filters and charge-pump PLL [2] loop filters.

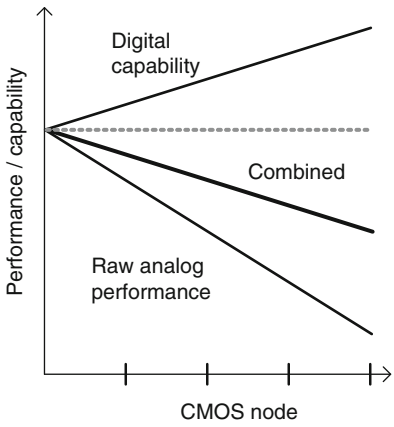

Fig. 3.2 Effect of CMOS process advancement on digital and, ultimately, RF performance

The above observation is graphically captured in Fig. 3.2. The raw analog performance, which is based on the traditional linear transistor operation, keeps on getting worse with each CMOS process node advancement in almost every aspect. On the other hand, the raw digital capability, in terms of processing sophistication and speed, is improving. An interesting question is whether the new powerful, yet inexpensive, digital logic and memory can compensate (through well-known techniques such as calibration, compensation and predistortion) for the increasing handicap of analog performance.

The unfortunate answer is generally "no". The raw performance degradation of RF circuits is much worse than the assistance the digital processing can offer. The chief reason for this negative answer is the sheer complexity of the transceiver component interaction. While it might be possible in an isolated case to calibrate or compensate for single parameter degradation, a degraded component typically affects multitude of parameters, which are very difficult or even impossible, within a given processing budget, to simultaneously calibrate. For example, an imperfection of active devices in an RX down-conversion mixer can simultaneously increase the leakage between the LO and input ports, which then increases dc offset at the mixer output, as well degrades the mixer's linearity in addition to skewing the delay between the I and Q paths. All these three system imperfections contribute to the signal distortion in a way that is difficult to isolate from each other. This makes the calibration algorithm disproportionately more complex or even unfeasible.

A quick survey of the most recent literature reveals no such impending doom and gloom. In fact, the RF performance of highly integrated system-on-chip (SoC)'s actually keeps on improving. The reason for this apparent paradox is the *changing* nature of the RF circuit design. Just like it has happened with the analog audio processing in the 1980s and 1990s, when new digitally-intensive techniques (oversampling, $\Sigma\Delta$ noise shaping, calibration, etc.) started being employed, the same level of sea change is being experienced now in the field of RF circuit design. Arguably, the first demonstrations of the new all-digital approaches to RF [7, 8]

were so revolutionary that they must have been perceived as threatening enough to the traditionally-minded RF design community, such that a frantic search for more evolutionary alternatives has been spurred. Even though the new Digital RF approach is now dominant in mobile phones, the analog-intensive alternatives still exist. However, their nature has been changed forever.

3.2 New Paradigm of RF Design in Nanometer-Scale CMOS

The author considers himself fortunate enough that his small group at Texas Instruments in Dallas, TX, USA, back at the end of 1999 was believed the first ever in the world to have tried to design RF circuits in deeply-scaled CMOS environment (130 nm CMOS node at that time). To put this into proper perspective: The design of RF circuits in any type of CMOS around the year 2000 was so uncommon in industry that it was generally met with incredulity and derision, and it took a few prominent researchers in academia [5, 9] to gradually change that negative perception. On top of that, our desire was not only to use CMOS for RF circuit design but rather its most advanced digital version for the purpose of single-chip radio integration. This general atmosphere of ignorance, negativity and avoidance outside of our immediate group has given us enough head start and secure a few years of development advantages. As a result, Texas Instrument's market share in RF has risen from virtually zero in 1999 to about 33% nowadays.

Our early attempt at designing RF circuits in advanced CMOS has made it clear that we were facing a new paradigm, which has allowed us to form a foundation of a new area of electronics: Digital RF. The new paradigm was first formulated in the author's 2002 Ph.D. thesis [10] (subsequently re-published as a 2006 Wiley book [11]) and is repeated below:

> In a deep-submicron CMOS process, time-domain resolution of a digital signal edge transition is superior to voltage resolution of analog signals.

In the good old days of analog IC design with the supply voltage of ± 15 V (yes! both positive and negative feeds simultaneously available), then 12 V, then 5 V, then 3.3 V, and finally 2.5 V, a large voltage headroom could be exploited for precise voltage tracking and setting of an analog waveform. Nowadays, with only 1.0–1.2 V, which needs to be spent on 500–600 mV of threshold voltage per each NMOS and PMOS transistor, there is little voltage headroom to perform any sophisticated analog processing. However, the MOS transistors are now extremely fast and can switch between V_{SS} and V_{DD} supply levels in almost no time (OK, 15–30 ps). Hence, the information can be tracked and processed as timestamps of sharp transitions between V_{SS} and V_{DD}.

Figure 3.3 further illustrates this point. The increasing level of noise makes the voltage resolution ΔV worse. Combined with the decreasing levels of supply voltage $V_{DD} - V_{SS}$, which lowers the maximum voltage swing V_{max}, the dynamic range $(V_{max}/\Delta V)$ of the signal gets lower.

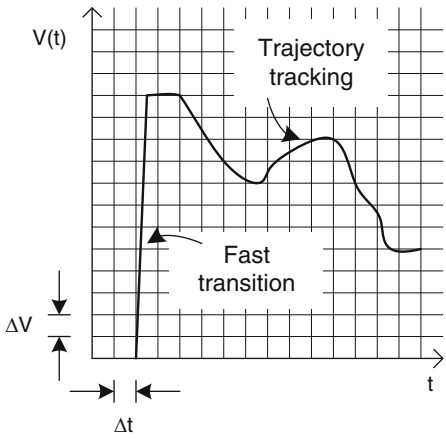

Fig. 3.3 Time-domain vs. voltage-domain view of a signal representation

Consider now the references available to IC designers. A typical tolerance of monolithic voltage/current sources or resistive/capacitative/inductive components (R/C/L) ranges from 0.5 to 10%. Trimming, heavily used in precision analog IC's, can bring down these tolerances to the 0.1–1% level, albeit at a high cost, which could virtually make it prohibitive for high-volume consumer products. At the same time, a mixed-signal IC would typically contain a crystal-stabilized reference clock with the tolerance of 1–100 ppm (parts per million), which is orders of magnitude better. It all means that the time reference already available to the analog/mixed-signal/RF designers has superior relative quality to the other components and the timestamps of level transition events could be used as a means of transmitting information. All the quantities are related through fundamental circuit equations, such as $i(t) = C\frac{dv(t)}{dt}$ and $v(t) = L\frac{di(t)}{dt}$. This is another argument for moving towards the time-domain operation. "It is time to use time..."

At the implementational level, the new paradigm means that a successful design approach in this environment would exploit this paradigm by emphasizing the following:

- Fast switching characteristics or high f_T (20 ps and 250 GHz in 40-nm CMOS process, respectively) of MOS transistors: high-speed clocks and/or fine control of timing transitions
- High density of digital logic (1 Mgates/mm^2) and SRAM memory (4 Mb/mm^2) makes digital functions and assistant software extremely inexpensive
- Ultra-low equivalent power-dissipation capacitance C_{pd} of digital gates leading to both low switching power consumption ($P_T = f \cdot C_{pd} \cdot V_{DD}^2$) as well as potentially low coupling power into sensitive analog blocks
- Small device geometries and precise device matching made possible by the fine lithography in order to create high-quality analog data converters

while avoiding the following:

- Biasing currents that are commonly used in analog designs (sometimes the digitally-controlled biasing current sources could be replaced by digitally-controlled resistors in which the MOS transistors operate in the linear mode).
- Reliance on voltage resolution with ever decreasing supply voltages and increasing noise and interferer levels.
- Nonstandard devices that are not needed for memory and digital circuits, which constitute majority of the silicon die area.

Despite the early misconceptions that the digitalization of RF would somehow produce more phase noise, spurs and distortion, the resulting digitally-intensive architecture is likely to be overall more robust by actually producing lower phase noise and spurious degradation of the transmitter chain and lower noise figure of the receiver chain in face of millions of active logic gates on the same silicon die, as repeatedly proven in subsequent publications [7, 8, 12, 13]. Additionally, the new architecture would be highly reconfigurable with analog blocks that are controlled by software to guarantee the best achievable performance and parametric yield. Another benefit of the new architecture would be an easy migration from one process node to the next without significant rework.

3.3 RF-SoC Landscape

Let us examine the landscape of RF system-on-chip (RF-SoC)'s based on the published literature. Table 3.1 shows the list of seven disclosures. They all came from commercial efforts involving large design teams so a reasonable effort to reduce area and power can be assumed.

The very first published report of an RF-SoC was in 2001 from Alcatel [14] targeting the Bluetooth standard. Its silicon area was 40 mm^2 in 250 nm CMOS. It was a significant commercial endeavor but, to the author's best knowledge, the chip never went into volume production. The second published RF-SoC [7] was from the author's former group in Texas Instruments (TI). It occupies only 10 mm^2 in 130 nm CMOS and is based on the presented Digital RF principles. It was put into volume production a few years earlier, which continues to this moment despite the fact that the original 130 nm architecture was subsequently fine-tuned to the 90-nm, then 65-nm and, most-recently, 45-nm CMOS nodes and adjusted for the polar TX modulation to handle the extended data rates (EDR) of 2 Mb/s and 3 Mb/s.

The third published RF-SoC and the first one targeting a cellular standard, was in 2006 from Infineon [15]. The GSM single-chip radio occupies 34 mm^2 in 130 nm CMOS and got created by combining Infineon's existing digital baseband (DBB) and transceiver (TRX) 130 nm chips. Remarkably, there is no mention of any digital assistance and the overall impression is that the RX-DBB integration exercise was rather hurried, thus giving little time to exploit the synergy. The RF/analog portion takes 13 mm^2, which is 38% of the total area. The fourth published RF-SoC [16]

Table 3.1 Published wireless RF-SoC's

	Company	Year	Wireless standard	CMOS node [nm]	SoC area [mm^2]	RF area [mm^2]	RF supply [V]	TX current [mA]	RX current [mA]	LO arch	TX arch	RX arch
[14]	Alcatel	2001	Bluetooth	250	40.1	10	2.5	52	41	ΣΔ CP-PLL	ana.-IQ	ana.-IQ
[7]	TI	2004	Bluetooth	130	10	3	1.5	25	37	ADPLL	dig.-FM	SC-IQ
[15]	Infineon	2006	GSM	130	34	13	2.5	90	120	ΣΔ CP-PLL	frac-PLL	ana.-IQ
[16]	Atheros	2006	PHS (1.9 GHz)	180	33	12	3.0/1.8	54	57	ΣΔ CP-PLL	ana.-IQ	ana.-IQ
[12]	TI	2008	GSM	90	24	3.8	1.5	47	56	ADPLL	dig.-polar	SC-IQ
[17]	Atheros	2008	Bluetooth v2	130	9.2	3	1.2	19.3	29.7	ΣΔ CP-PLL	ana.-polar	ana.-IQ
[18]	Atheros	2008	2x2 .n WLAN	130	36	11	3.3/1.2	280	310	ΣΔ CP-PLL	ana.-polar	ana.-IQ

was also in the same year but targeted the Personal Handy-Phone System (PHS) standard in the 1,900 MHz frequency band used mainly in Japan and in parts of China. It occupies 35 mm^2 SoC in 180 nm CMOS and RF/analog area is 11 mm^2, which is about 30% of the total.

The fifth RF-SoC [12] and the first implemented in a nanometer-scale CMOS (feature size less than 100 nm), was in 2008 from the author's group in TI targeting GSM and based on the second-generation of the Digital RF principles. The silicon area is 24 mm^2 in 90 nm CMOS, 3.8 mm^2 of which is used by RF/analog, which makes it only 16%.

In the same year of 2008, there were two other disclosures, both from Atheros and both using 130 nm CMOS. The first [17] is targeting the EDR version of Bluetooth, and the second [18] is targeting the 2x2 MIMO wireless LAN. The silicon area is 9.2 mm^2 and 36 mm^2 and the RF/analog occupies 33% and 31%, respectively.

All the seven RF-SoC's, except for the two from TI based on the Digital RF principles, are based on the conventional analog-intensive architecture: The frequency synthesizer comprising the LO is build using a charge-pump PLL in which the fractional frequency resolution is obtained through $\Sigma\Delta$ dithering of the modulus divider. The transmitter is either analog I/Q or analog polar topology, while the receiver is a typical continuous-time mixer-based architecture. In contrast, the digitally-intensive implementations by TI [7, 12] use all-digital phase-locked loop (ADPLL) for the LO, digital polar modulator for the TX and switched-cap based discrete-time RX. All of them, however, disclose employment of the digital assistance of RF (except for [15]).

Table 3.1 clearly shows the CMOS scaling trend when implementing fully-integrated RF radios, whether using the traditional analog-intensive or new digital-intensive approaches. The analog-intensive approaches, however, do not fully benefit from scaling. Their silicon area and power consumption (RF supply times TX/RX current) tend to be much higher. Non-cellular wireless applications require less stringent RF performance but the lower supply voltage of core transistors appears to be achievable only with Bluetooth, which is considered the least demanding of all popular standards. As no publications for single-chip radios in nanoscale CMOS have yet been reported for that traditional approach, their scaling effectiveness is yet to be seen. It should be noted that fair comparison of the proposed techniques is best afforded against other SoC radios with predominantly digital content, which typically allocate only 15–40% of the die area to the RF transceiver functionality. Production issues, such as yield loss due to parametric variability of analog/RF circuits, test coverage, required time and cost of RF test, calibration and compensation [19], are not appreciated to the same degree as with testchips and stand-alone RF transceivers but can significantly impact the SoC design style and architectural choices.

The examples of published commercial RF-SoC's consistently reveal that the RF portion of entire SoC is only 15–40%, as shown in Fig. 3.4. It means that the majority of the area is occupied by the digital logic and memory in order to implement the digital baseband together with various controller and application

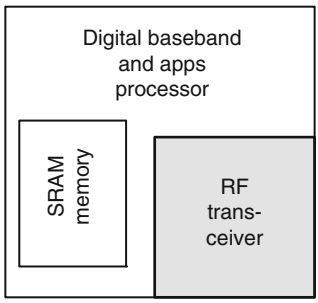

Fig. 3.4 RF transceiver as part of a larger RF-SoC

processor functionality. For this reason, the logic and memory determine the technology choice and it is rather not favorable to the linear RF operation.

3.4 Digital RF Processor (DRP^{TM})

The Digital RF principles presented in this chapter have been used in TI to develop three generations of a commercial Digital RF Processor (DRP^{TM}): single-chip Bluetooth [7], GSM [12] and EDGE [13] radios realized in 130-nm, 90-nm and 65-nm digital CMOS process technologies, respectively. Figure 3.5 shows the chip micrographs. It is estimated that the cellular market share of DRP is currently 33% of the worldwide annual production. In addition, TI's high-volume wireless connectivity RF-SoC's in 90 nm, 65 nm and 45 nm CMOS are designed according to these principles. When combined with TI's competitors' products also having embraced these principles, it appears that Digital RF is now the predominant architecture found in entry-level and feature cellular phones.

Figure 3.6 highlights the common RF-SoC architecture of DRP products with added features specific to the cellular radio. At the heart of the transceiver lies the all-digital PLL (ADPLL) [8], generating local oscillator (LO) and almost all other clocks, including those for the DBB. The ADPLL-based transmitter employs the polar architecture with all-digital phase/frequency and amplitude modulation paths. The receiver [20] employs a discrete-time architecture in which the RF signal is directly sampled and processed using analog and digital signal processing techniques. The antenna RF input signal is amplified and converted into the current domain by a low noise transconductance amplifier (LNTA). The RF current is then directly sampled or mixed to zero-IF or very-low-IF in the charge domain. The signal is then filtered and converted into the digital domain for further conditioning. A digitally-controlled crystal oscillator (DCXO) generates a high-quality basestation-synchronized frequency reference such that the transmitted carrier frequencies and the received symbol rates are accurate to within 0.1 ppm. A power management system consists of a bandgap generator and multiple low drop-out (LDO) linear regulators to supply voltage to various radio subsystems

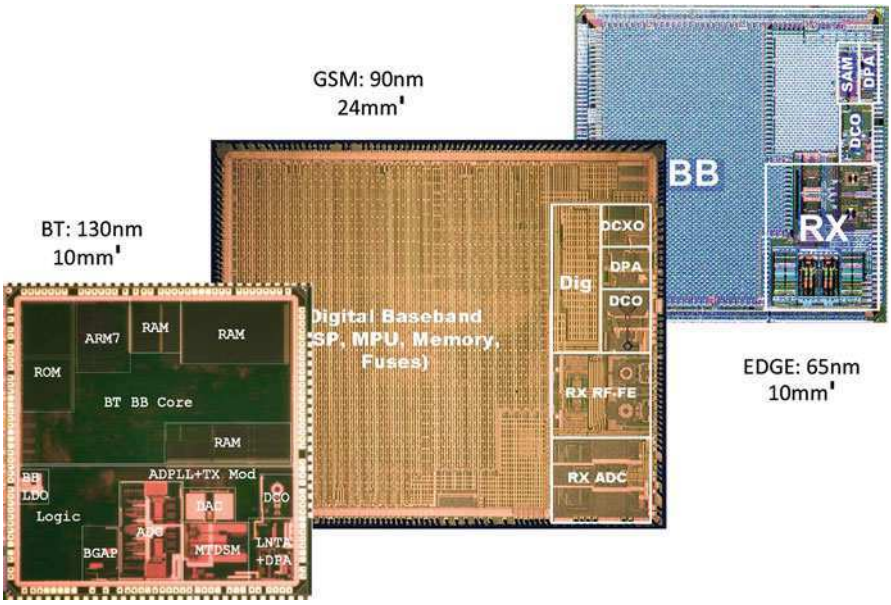

Fig. 3.5 Chip micrographs of the commercial single-chip RF-SoC's employing three generations of DRP: (*left-to-right*) 130 nm Bluetooth; 90 nm GSM; and 65 nm GSM/GPRS/EDGE

as well as to provide good noise isolation between them. Various calibration and compensation procedures are exercised to keep the transceiver performance at optimum irrespective of the process and environmental conditions. One such example is a periodic "just-in-time" compensation of the DCO gain variations [21]. An RF built-in self-test (RF-BIST) [19] executes an autonomous transceiver performance and compliance testing of the GSM standard [22]. The embedded processor [23] handles various TX and RX process calibration, voltage and temperature compensation, sequencing and lower-rate datapath tasks and encapsulates the transceiver complexity in order to present a much simpler software programming model. The data and high-level control is routed from/to digital baseband processor via data bus router. The transceiver is integrated with the digital baseband, SRAM memory in a complete system-on-chip (SoC) solution.

3.4.1 Patents on Digital RF

To give an indication of the intellectual property (IP) situation, the most early Digital RF patents are listed in Table 3.2. Since TI was years ahead of anyone else in researching this area (see Sect. 3.2), it owns most of the early fundamental patents. The situation nowadays, however, is entirely different. A great majority of the newly

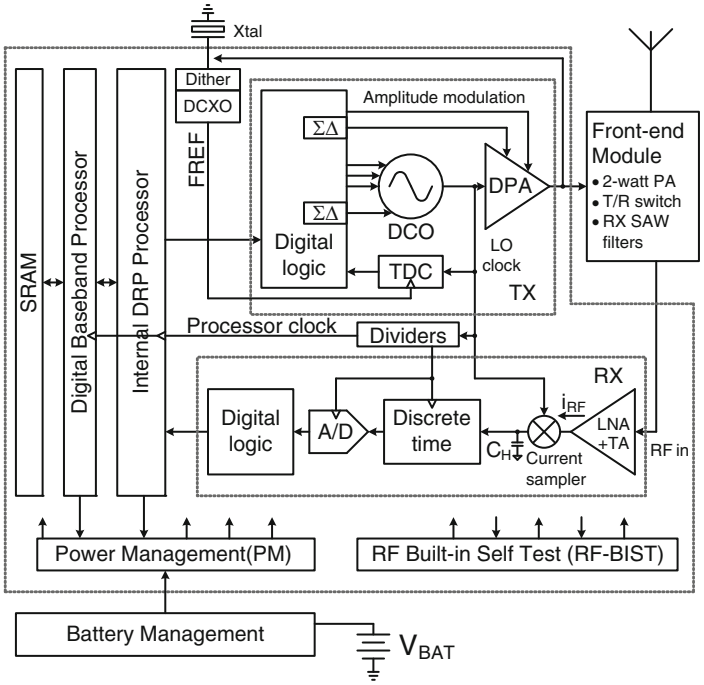

Fig. 3.6 Single-chip GSM cellular radio based on the second generation of DRP. Script Processor communicates with the digital baseband processor and oversees the entire RF transmitter and receiver functionality

Table 3.2 Early digital RF patents (TI)

US patent	Filing date	TI inventors	Title
6,326,851	2000-06-26	R.B. Staszewski, D. Leipold	Phase-Domain ADPLL
6,429,693	2000-06-30	R.B. Staszewski, D. Leipold	TDC-ADPLL
6,658,748	2000-10-05	D. Leipold, R.B. Staszewski	DCO
6,809,598	2000-10-24	R.B. Staszewski, D. Leipold, K. Maggio	ADPLL FM
6,414,555	2001-02-22	R.B. Staszewski, D. Leipold, K. Maggio	ADPLL w/DDS
6,959,049	2001-04-06	R.B. Staszewski, D. Leipold	Direct-sampling mixer

issued patents in the area of Digital RF are owned by other companies, as Table 3.3 indicates. With the total count of a few hundreds, the Digital RF IP ownership is now mostly spread around the world. This is an indication of a dynamically growing and very healthy industry and parallels the historical development of IC chip. Even though TI invented the IC chip and held the fundamental patents, it obviously did not hurt its fantastic commercial growth. In fact, only a small minority of the patents related to IC nowadays belongs to TI.

Table 3.3 Most recent US patents (or patent publications) related to Digital RF

US patent	Issue date	Company	Area
7,917,797	2011-03-29	Xilinx	ADPLL
7,911,248	2011-03-22	ETRI	DCO
7,907,023	2011-03-15	Panasonic	ADPLL
7,888,973	2011-02-15	Marvell	TDC
7,884,751	2011-02-08	STARC/Japan	TDC
7,869,555	2011-01-11	STM	ADPLL
7,868,672	2011-01-11	Qualcomm	ADPLL
7,859,343	2010-12-28	ITRI/Taiwan	ADPLL
7,847,642	2010-12-07	Infineon	DCXO
7,848,266	2010-12-07	ADI	ADPLL
2010/0301953	2010-12-02	Panasonic	ADPLL
2010/0295590	2010-11-25	Toshiba	TDC
7,812,644	2010-10-12	Samsung	TDC
7,808,418	2010-10-05	Qualcomm	TDC
7,592,874	2010-09-22	Infineon	ADPLL
7,791,428	2010-09-07	Mediatek	ADPLL
7,777,578	2010-08-17	Infineon	DCO
7,772,929	2010-08-10	Infineon	DCO
7,772,900	2010-08-10	IBM	ADPLL
2010/0195779	2010-08-05	Toshiba	ADPLL
7,759,993	2010-07-20	Qualcomm	ADPLL
7,750,701	2010-07-06	IBM	ADPLL
2010/0141316	2010-06-10	STM	ADPLL/TDC
7,728,686	2010-06-01	Mediatek	ADPLL/DCO
7,729,445	2010-06-01	Intel	DPA
7,719,366	2010-05-18	Sony	ADPLL
7,714,668	2010-05-11	Panasonic	TDC
7,715,515	2010-05-11	Ericsson	DCO
7,706,496	2010-04-27	Skyworks	ADPLL/TDC
7,696,830	2010-04-13	Toshiba	ADPLL/DCO
7,696,829	2010-04-13	Infineon	ADPLL
7,692,500	2010-04-06	Marvel	DCO
7,688,145	2010-03-30	Toshiba	DPA
7,688,126	2010-03-30	Infineon	TDC
2010/0066421	2010-03-18	Qualcomm	ADPLL
2010/0066417	2010-03-18	NXP	ADPLL
7,671,658	2010-03-02	Panasonic	SC mixer

3.5 All-Digital Phase-Locked Loop (ADPLL)

As mentioned in Sect. 3.1.1, every wireless system requires at least one local oscillator (LO), realized as a frequency synthesizer, to perform frequency translation between baseband and RF frequencies.

The frequency synthesizer takes a frequency reference (FREF) clock of frequency f_R (typically 8…52 MHz) and generates a variable frequency f_V at the multi-GHz RF output according to either an integer or fractional frequency multiplication ratio $N = f_V / f_R$ or frequency command word (FCW), where FCW $\equiv N$. The FREF source is usually built as a tunable crystal oscillator, which features an excellent long-term accuracy and stability. Due to relatively high cost of resonating crystal slabs, which are also bulky and require special packaging, there undergoes an intensive research for solid-state alternatives, such as RC-based oscillators with accurate temperature compensation as well as MEMS-based resonators. To the author's best knowledge, these emerging solutions are not yet mature enough to replace the decades-old proven crystal-based solutions in volume production of consumer products.

In older process technologies, the frequency synthesizer has been traditionally based on a charge-pump PLL [2], as shown in Fig. 3.7a, but this architecture is not easily amenable to scaled CMOS integration. Due to the low supply voltage constraint and poor drain-source dynamic resistance r_{ds} of MOS transistors, the current sources of the charge pump are now far from ideal. Also, the loop filter capacitor needs to be large to suppress reference spurs of the charge pump. While external capacitors are typically acceptable in low-complexity IC's, more sophisticated SoC's would not tolerate the associated extra input/output (I/O) interface, routing and signal integrity degradations. If realized as a metal-insulator-metal (MIM) capacitor, its size could be prohibitively large. MOS capacitors offer about 10 times area density improvement but the leakage current, which is due to gate electron tunneling, is getting worse with each process node. The leaky capacitor would introduce an equivalent parallel resistance whose value strongly depends on temperature, thus changing the loop characteristics. Efforts have been made to extend the architecture's lifetime by, for example, replacing the loop filter capacitor with a digital integrator or accumulator [24]. Since the capacitor's input and output are analog, the replacing accumulator needs to be preceded by an ADC and followed by a DAC.

Moreover, the charge-pump PLL architecture suffers from high level of reference spurs generated by the correlative phase detection method, which require better filtering and thus slower loop transients that degrade frequency-settling times. To relax this tradeoff, a fractional-N PLL architecture with $\Sigma\Delta$ dithering of the clock division ratio is often used but at a cost of higher quantization noise. Furthermore, ensuring wide linear tuning range of a VCO is very difficult in low-voltage technologies [10]

The new ADPLL [10, 11] frequency synthesizer architecture that is amenable to the scaled CMOS technology and is free of the above problems is presented in Fig. 3.7b. It is built from the ground up using digital techniques that exploit the new paradigm described in Sect. 3.2. It truly operates in the phase domain, which was first proposed by Kajiwara and Nakagawa [25]. This is in clear contrast to the traditional charge-pump PLL architecture, in which the phase domain operation is only a small-signal approximation under the locked loop condition [2].

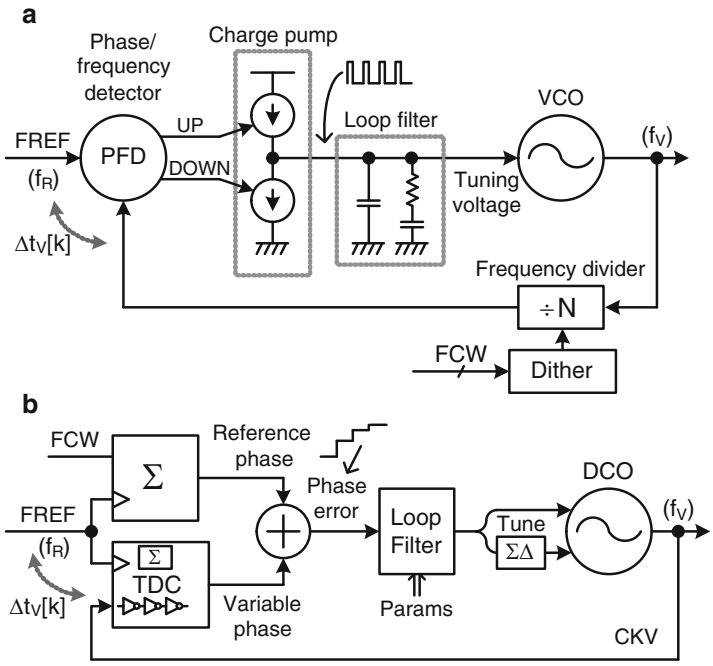

Fig. 3.7 RF frequency synthesizers: (**a**) conventional charge-pump PLL; (**b**) all-digital phase-domain PLL based on time-to-digital converter (TDC) and digitally-controlled oscillator (DCO). $FCW \equiv N$ is a fractional frequency division ratio

3.5.1 ADPLL Phase-Domain Operation

Figure 3.8 explains the phase domain operation of the ADPLL. The frequency reference information is wholly contained in the transition times (i.e., timestamps) of the frequency reference (FREF) clock. Of the two possible transition types, only rising clock edges are used here. Likewise, the timing information of the high-frequency variable clock (CKV) is contained in its rising edge timestamps. For the sake of illustration, the frequency command word (FCW), denoting the *expected* frequency multiplicative ratio, is 3.2. Since the oscillation time period is an inverse of the oscillating frequency, there will be 3.2 clock cycles of CKV per single cycle of FREF. Also, we assume the initial phase to be zero (i.e., FREF and CKV rising edges are aligned at time zero), although, in general, it does not need to be the case.

The phase domain operation is based on numerically calculating the phase error $\phi_E[k]$, which is a difference between the reference phase $R_R[k]$ and variable phase $R_V[k]$. The unit of the phase calculation, also called unit interval (UI), is the CKV clock period. Hence, the reference phase signifies the *expected* number of CKV cycles from the time zero (i.e., calculated as a summation of FCW:

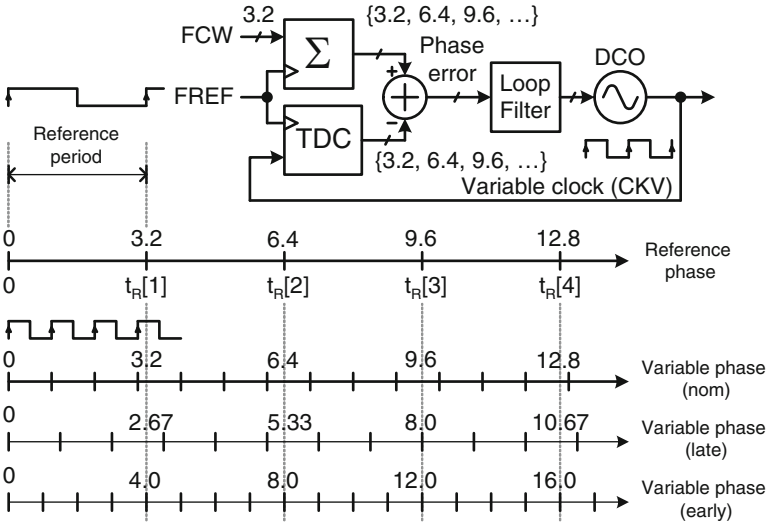

Fig. 3.8 Principle of the phase-domain operation

$R_R[k] = \sum FCW[k]$), whereas the variable phase signifies their *actual* number. In other words, the difference between the actual and ideal count of CKV cycles at each reference edge is a measure of phase *departure* or phase error, $\phi_E[k] = R_R[k] - R_V[k]$. The phase error then adjusts the DCO frequency and phase in the negative feedback manner.

A small inconsistency in the reasoning logic might possibly be noticed here. The variable clock CKV period, rather than the more stable FREF period, is the unit measure of the $R_R[k]$ and $R_V[k]$ phase quantities even though the CKV is *subject to change* due to noise and possible change in FCW (due to intended frequency modulation). Despite this apparent paradox, the system works properly since the error correction mechanism is the *difference* between these two phase quantities. As an example, the phase error needs to go higher (i.e., DCO needs to speed up), if the variable phase gets lower (i.e., DCO gets slower) or the reference phase gets higher (i.e., more CKV cycles per FREF cycle). Assuming the FREF clock is stable, as it is supposed to be, and FCW is constant, both of these cases are equivalent to the DCO getting slower. In case the FCW increases, the DCO is *requested* to speed up.

3.5.2 ADPLL Implementation

Block diagram of Fig. 3.7b is now redrawn in Fig. 3.9 with more implementation details. The DCO shows not a single but actually three tuning word inputs to separately control the three varactor banks: process, voltage, temperature (PVT) centering; acquisition and tracking. The PVT bank ("P") re-centers the DCO natural

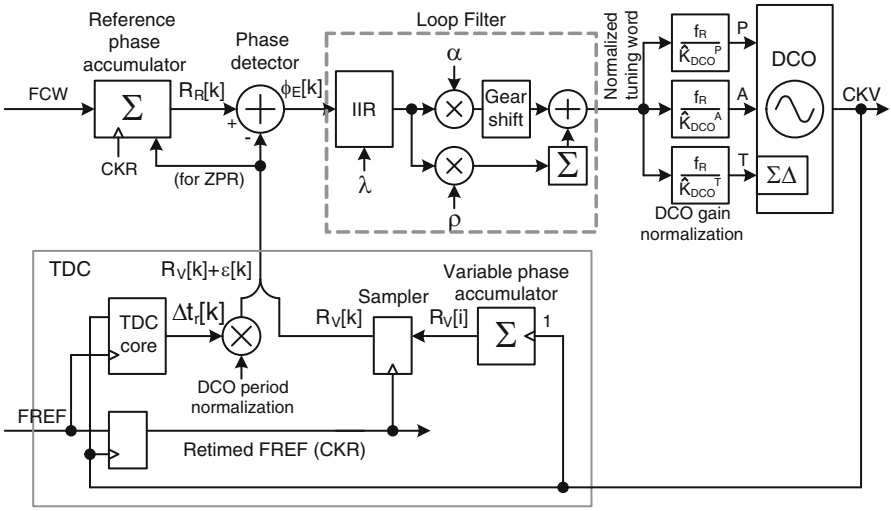

Fig. 3.9 Detailed block diagram of the ADPLL

frequency to the middle of the selected frequency band. The acquisition bank ("A") performs channel selection by quickly settling to the neighborhood of the desired frequency. The tracking bank ("T") is the one actually used during the mission-mode transmission or reception. The ADPLL quickly transverses the P/A/T varactor banks with progressively finer frequency steps (GSM example: 4 MHz, 200 kHz and 12 kHz, respectively) while significantly narrowing down the loop bandwidth at each step. This way, the final loop bandwidth, and thus settling time, can be extremely fast (5–20 μs) and largely independent from the initial frequency difference. Optimized settling times of 5 μs and 7 μs are reported in [26] and [27], respectively. To maintain a certain control of the ADPLL filtering characteristics, each of the three tuning inputs has its own DCO gain estimation normalizing multiplier $f_R/\widehat{K}^X_{DCO}$, where X = P, A, T. The accuracy of K^P_{DCO} and K^A_{DCO} is not very critical. For example, 10% error of their value can lead to only 10% change in the loop bandwidth and acquisition time.

The loop filter consists of a $4th$-order IIR filter followed by a proportional-integral (PI) controller that includes the proportional gain factor α and integral gain factor ρ. The attenuator factor α establishes the PLL loop first-order filtering characteristic: $f_{BW} = \alpha \cdot f_R/2\pi$, where f_{BW} is a 3-dB cut-off frequency of the closed PLL loop. For example, in a Bluetooth operation, where the IIR filter is not used, the α value is changed several times during the frequency locking with an initial $\alpha = 2^{-3}$ and final $\alpha = 2^{-8}$ values resulting in $f_{BW} = 259$ kHz and $f_{BW} = 8$ kHz, respectively, for the f_R = 13 MHz reference frequency. The final value of α was chosen to be the best tradeoff between the phase noise of the reference input and the DCO phase noise during the transmit (TX) and receive (RX) operations. The integral loop factor $\rho = 2^{-18}$ is activated shortly after the loop is settled. It switches the PLL

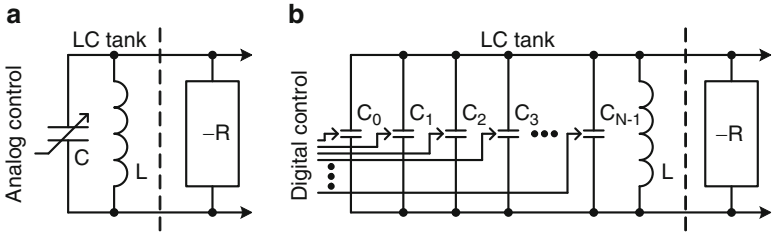

Fig. 3.10 LC tank based-oscillators: (**a**) conventional with analog control; (**b**) with all-digital control. The negative resistance $-R$ perpetuates the lossy LC tank resonance

characteristic from type-I to type-II with the damping factor $\zeta = \frac{1}{2}(\alpha/\sqrt{\rho}) = 1$ in order to effectively filter out the oscillator flicker noise, which tends to be quite high in a scaled CMOS.

3.5.2.1 Digitally-Controlled Oscillator

At the heart of the ADPLL lies a digitally-controlled oscillator (DCO). It is based on an LC-tank with a negative resistance to perpetuate the oscillation – just like the traditional voltage-controlled oscillator (VCO) on Fig. 3.10a. However, there is a significant difference in one of the components: instead of a continuously-tuned varactor (variable capacitor), the DCO now uses a large number of binary-controlled varactors (Fig. 3.10b), as first proposed in [28]. Each one can be placed in either high or low capacitative state. The composite varactor performs a digital-to-capacitance conversion (DCC). Since the varactors, i.e., the DCO input, are digitally controlled, and since the output clock at multi-GHz frequencies is almost perfectly digital (the rise and fall times could be as fast as 20 ps), the loop around the DCO, which adjusts its phase and frequency, could be now fully digital, as first proposed in [29].

The finest varactor step size made possible by the fine lithography is on the order of 40 aF (i.e., 40E-18 F), which corresponds to 12 kHz frequency step size at the 2 GHz DCO output. This is equivalent to a fine control of about 250 electrons leaving and entering the LC-tank. Unfortunately, this fine control is not sufficient for any commercial wireless standard, so dithering is used that improves the *time-averaged* capacitative resolution. A typical realization uses a second-order MASH $\Sigma\Delta$ modulator running at 2 GHz/8 clock rate with 8 fractional input bits will produce the sufficiently-fine open-loop resolution of 12 kHz/256 = 45 Hz, which is now equivalent to about one electron.

Figure 3.11 shows a simplified schematic of the DCO core that operates in the 3.2–4.0 GHz range. The tuning control is split into several banks of varying degree of frequency step size and range: coarse d^P for process, voltage and temperature (PVT) calibration, medium d^A for channel acquisition and fine d^T for tracking of the oscillator drift. The d^P frequency range is the largest since it has to cover all the frequency bands and margin for the oscillator variability. The oscillator phase noise

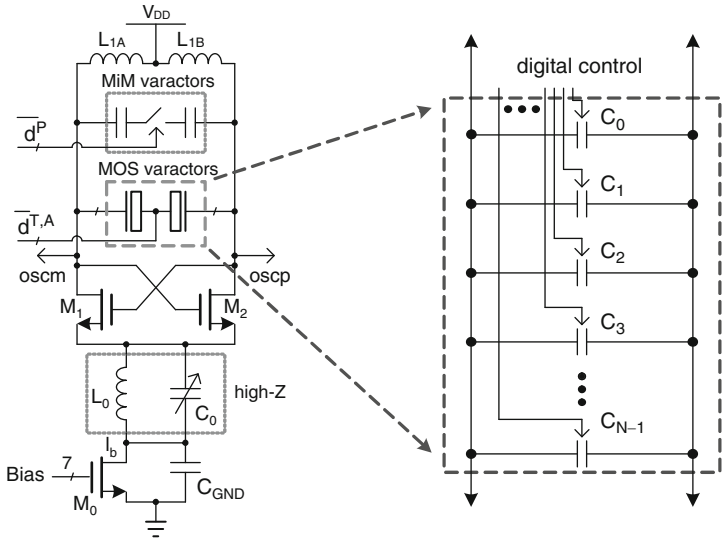

Fig. 3.11 Oscillator core and the varactor state driver array

is proportional to the dissipated current, which is established by the 7-bit "bias" control. The capacitor banks are built using MIM and MOS varactors. In agreement with the Sect. 3.2 principle of avoiding biasing currents, the M_0 transistor array operates in linear region instead of in saturation. The current is set through automatic calibration at a minimum value at which the oscillator still produces acceptable RF phase noise.

The DCO is a highly-linear replacement of the traditional VCO. The fine frequency resolution is achieved by $\Sigma\Delta$ dithering of its finest unit-weighted variable capacitors (varactors) using the high-speed down-divided DCO clock, as shown in Fig. 3.12. The tuning word is a fixed-point number with the integer part directly controlling the number of active unit-weighted binary-controlled varactors. The fractional part is fed to the $\Sigma\Delta$ modulator, which produces an integer stream whose average value is equal to that of the fractional input.

3.5.2.2 Time-to-Digital Converter (TDC)

The TDC, as shown in Fig. 3.13, generates the variable phase or timestamps of the FREF edges in the units of the DCO clock period [30]. The variable phase is a fixed-point digital word in which the fractional part is measured with a resolution of an inverter delay (less than 20 ps and 10 ps in 90-nm and 40-nm CMOS, respectively) by means of the TDC core, as shown in Fig. 3.14a. The DCO variable clock, CKV, gets delayed by the string of inverters or buffers, whose outputs are sampled with the rising edge of FREF. Thus obtained 48-bit TDC core output forms a

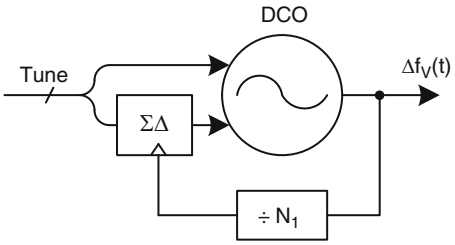

Fig. 3.12 Actual realization of the DCO with resolution improvement through a $\Sigma\Delta$ modulator clocked by the down-divided DCO output clock

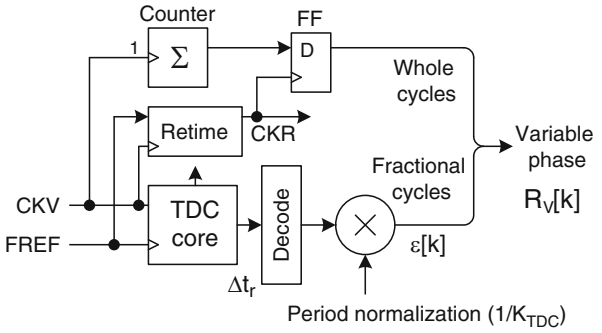

Fig. 3.13 TDC system with large dynamic range

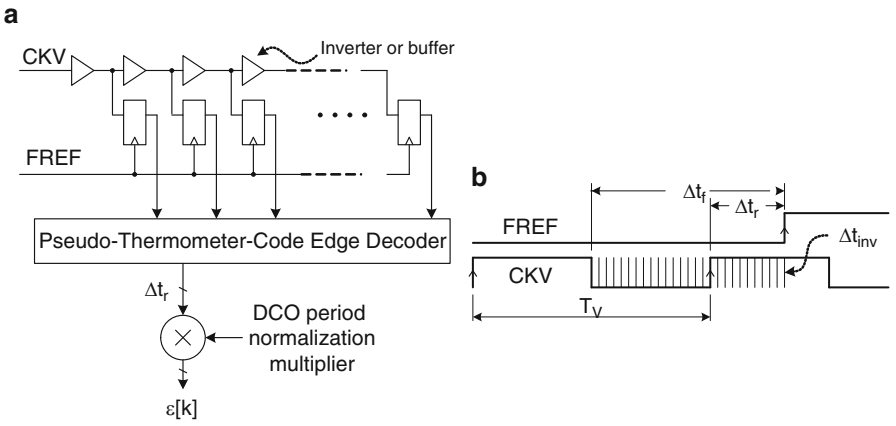

Fig. 3.14 Time-to-digital converter (TDC) core: (**a**) structure; (**b**) quantization of the timing difference between the DCO and FREF edges. The integer counter of DCO edges is not shown

pseudo-thermometer code, which is then converted to binary and normalized to the CKV period, T_V. The number of inverters is set to cover one T_V. To arbitrarily increase the dynamic range, the CKV edge counter with a sufficient wordlength is added, thus contributing to the integer part of the variable phase. The fixed-point TDC output timestamp consists of the sampled CKV edge count (integer part) and the T_V-normalized delay from CKV to FREF (fractional part). The time difference

between the two FREF events is the difference between the two consecutive outputs. In PLL applications, the absolute timestamps (phase) are more useful than the time difference (instantaneous frequency). Also, the reference edge locations are quite predictable, so the power is significantly saved by gating off the TDC activity during 95% of the time between the reference edges. To avoid metastability between the counter and the TDC core, FREF resampling by the opposite phases of CKV was used [10].

The actual timestamps $R_V[k]$ are compared to the ideal timestamps or the reference phase $R_R[k]$, which is calculated as a summation of FCW: $R_R[k] = \sum FCW[k]$. The timing departure or the phase error $\phi_E[k] = R_R[k] - R_V[k]$ is filtered, and adjusts the DCO in a negative feedback manner.

Since the conventional phase/frequency detector and charge pump are replaced by the TDC, the phase-domain operation does not fundamentally generate any reference spurs thus allowing for the *digital* loop filter to be set at an optimal performance point between the reference phase noise and the oscillator phase noise.

Because of the full digital nature of the phase error correction, sophisticated control algorithms through a dynamic change of the loop filter parameters (refer back to Fig. 3.7b) could be employed, which would not have been feasible with conventional architectures.

1. Dynamic gear shifting of the ADPLL bandwidth to speed up the frequency settling [31] and to respond to unexpected and expected disturbances in the SoC, such as ramping up the power amplifier and DBB, keyboard or display activities.
2. Adaptable characteristic of the ADPLL loop depending on the communication channel conditions or quality of the DCO and FREF clocks.
3. Dynamic change of the ADPLL loop characteristics, such as dynamically switching from type I to type II loop after the settling is complete.

3.6 All-Digital Transmitter

Figure 3.15 shows an RF transmitter formed as an extension of the ADPLL in Fig. 3.7b. Naturally, it is also amenable to the nanometer-scale CMOS technology. It performs the complex modulation in polar domain [7, 8] by utilizing two RF digital-to-"analog" converters (RF-DAC)'s: (1) the ADPLL-based digital-to-frequency converter (DFC); and (2) digital-to-RF-amplitude converter (DRAC) based on a digital power amplifier (DPA). In the former, the analog quantity is the frequency deviation from the RF center frequency, whereas in the latter it is the RF amplitude or envelope.

Transmit symbols, created from the user data, get pulse-shaped filtered in order to constrain the modulated carrier bandwidth to that of a given wireless standard. They are then converted from the I/Q to the polar domain. The resulting frequency command word (FCW) and amplitude control word (ACW) data samples drive the DFC and DRAC, respectively.

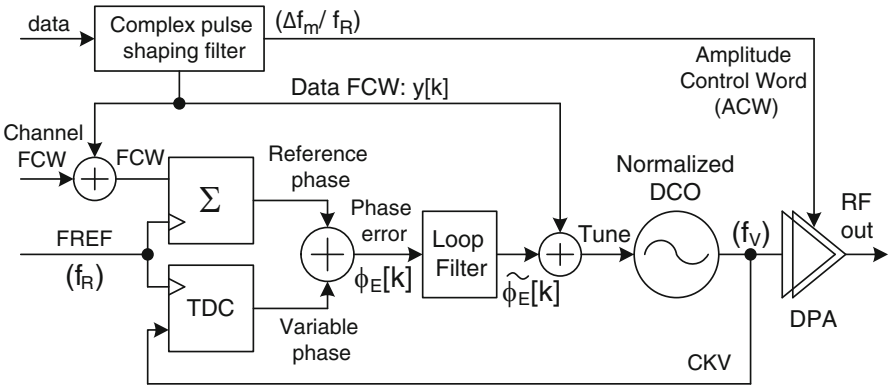

Fig. 3.15 ADPLL-based polar transmitter

The DFC architecture of Fig. 3.15 is fully digital and takes advantage of the wideband frequency modulation capability of the ADPLL by adjusting its digital FCW. The modulation method is an exact digital two-point scheme, with one feed directly modulating the DCO frequency deviation while the other compensating for the developed excess phase error. The DCO gain characteristics are constantly calibrated through digital logic to provide the lowest possible distortion of the transmitted waveform [21]. The DFC architecture will be described in detail in Sect. 3.6.2.

3.6.1 Digital Power Amplifier

The digital power amplifier (DPA) circuit, shown in Fig. 3.16, which acts as an RF-DAC in general and as a digital-to-RF-amplitude converter (DRAC) in particular, is used for the power ramp as well as amplitude modulation in more advanced modulation schemes, such as the extended data rate (EDR) mode of Bluetooth, EDGE or WCDMA. The DPA operates as a near-class-E RF power amplifier and is driven by the square wave output of the DCO. A large number of core NMOS transistors are used as on/off switches and are followed by a matching network that interfaces with an antenna or an external power amplifier, such as one providing 2 watts in GSM. The number of active switches is controlled digitally and establishes the instantaneous amplitude of the output RF envelope. Fine amplitude resolution is achieved through high-speed $\Sigma\Delta$ transistor switch dithering. Despite the high speed of digital logic operation, the overall power consumption of the transmitter architecture is lower than that of architectures to date.

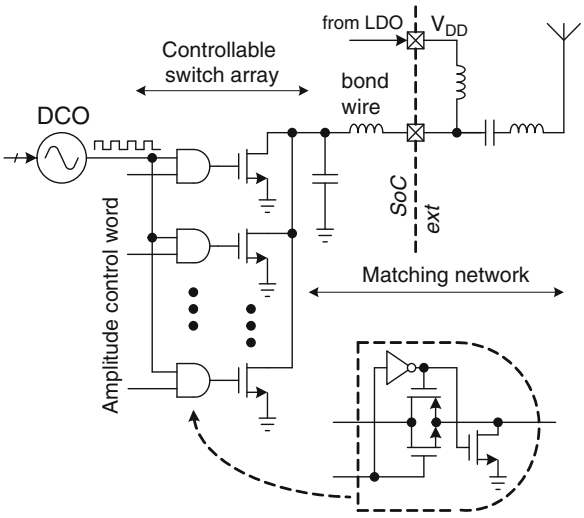

Fig. 3.16 Digital power amplifier (DPA) acting as a sort of an RF-DAC

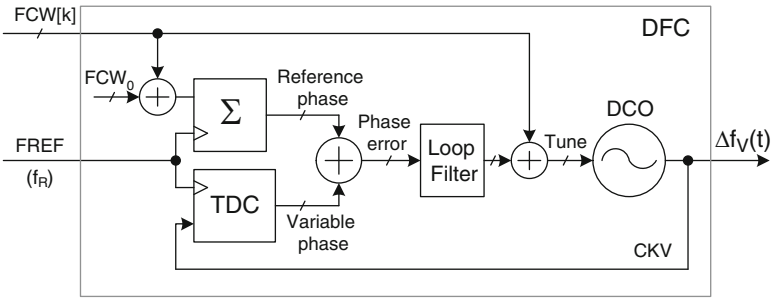

Fig. 3.17 RF digital-to-frequency converter (DFC) realized using a digitally-controlled oscillator (DCO)

3.6.2 ADPLL-Based Multirate Frequency Modulator

3.6.2.1 Towards Multirate ADPLL Operation

The DFC part of Fig. 3.15 is now redrawn as Fig. 3.17. It has been proposed [10, 11] for RF wireless applications that require low amount of spurious tones and phase noise (RF equivalent of jitter) as well as low power consumption. The new architecture is based on a digitally-controlled oscillator (DCO). Unfortunately, the free-running DCO would invariably exhibit wander or random walk of its phase with the expected variance approaching infinity [32]. Therefore, the DCO requires adjustment of its slowly varying wander (lower frequency components of its phase noise) with the stable frequency reference (FREF). The adjustments are obtained by forming a negative-feedback loop around the DCO. The higher

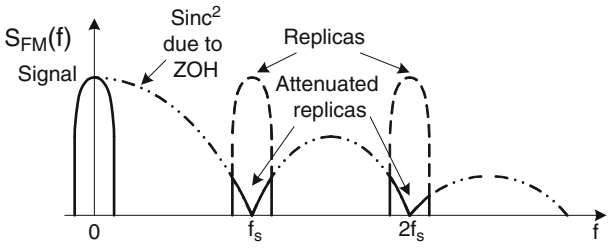

Fig. 3.18 Spectral replicas of a discrete-time FM signal and their filtering through sinc response of a ZOH

frequency components of the phase noise, which are beyond the loop bandwidth, will not be corrected. However, these components of a typical LC-tank oscillator can be made sufficiently low.

The closed-loop is built using an all-digital phase-locked loop (ADPLL) architecture. As discussed above, it comprises a time-to-digital converter (TDC) to estimate the variable phase; an FCW accumulator to calculate the reference phase; an arithmetic subtractor to calculate the phase error based on the reference phase and variable phase; the loop filter to control the ADPLL bandwidth and transfer function characteristic.

The ADPLL has a natural wideband FM capability. It is realized as a two-point modulation scheme. One feed directly modulates the DCO, while the other feed is compensating and prevents the modulating data from affecting the phase error. For this to work properly, the DCO needs to have a normalized gain $K_{DCO} = f_R$/LSB, where f_R is the reference frequency of FREF. Estimating K_{DCO} is relatively straightforward in ADPLL. The modulating transfer function is flat from dc to $f_R/2$ in z-domain and has only sinc-type response in s-domain caused by the DCO zero-order hold interface. Due to the lack of the continuous-time filtering, this will result in signal replicas at multiplies of the sampling rate f_s (here, $f_s = f_R$), as shown in Fig. 3.18.

The preferred sampling rate for GSM/EDGE transmitters is typically over 200 MHz (e.g., $N_1 > 8$) in order to spread the quantization noise, due to the limited resolution, over enough frequency range. Non-cellular transmitters typically have some additional constraints, such as coexistence with cellular host systems. For example, using $N_1 = 4$ or 8, does not work well for the Bluetooth 2.4 GHz f_0 carrier, since the $f_0 \pm 2 \cdot f_0/8$ replica energy could fall into the 1.8 GHz cellular band. Running the $\Sigma\Delta$ modulator at the $f_0/6$ rate avoids this problem.

Since the modulating samples are clocked at f_R, the ADPLL of Fig. 3.17 cannot handle the frequency content over $f_R/2$, which is $\leq$26 MHz, based on the above discussion. To make the data sampling rate independent from f_R and further push the replicas' energy beyond any protected frequency band, a new multirate architecture of Fig. 3.19 is proposed.

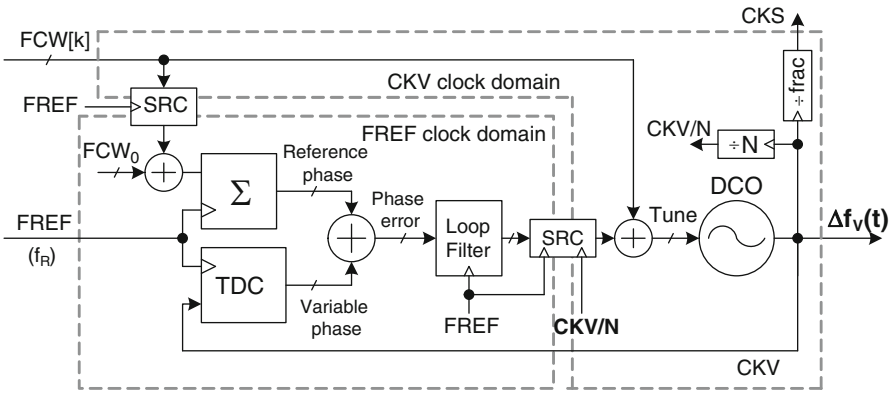

Fig. 3.19 Multirate DFC to handle modulation sampling rates higher than the FREF

The phase error detecting and filtering part of the ADPLL still runs at f_R rate. This is natural since the FREF clock is the only source here that provides the long-term super-stable timing reference to correct the slowly drifting DCO phase. Performing the phase error operations at a higher rate would not make sense. The phase error samples are filtered and upsampled to the f_V/N rate, where f_V is the variable frequency of the DCO and N is a small integer (preferably a power-of-two number). They are then merged with the modulating data of the same rate. The modulating data FCW[k] could be as high as 100's of MHz thus easily covering the most demanding modulation standards, such as LTE with I/Q 20 MHz channel bandwidth. Note that the I/Q signal conversion into ρ and θ polar components significantly expands the bandwidth [34], but techniques, such as [33], could be used to lessen that effect.

The two functional parts of the ADPLL-based frequency modulator: the phase error calculator and data modulator, have their own separate clock domains: FREF and CKV, respectively. Since their frequency relationship is a time-variant fractional number, their mutual interfaces require sampling rate converters (SRC). The SRC for the phase error is either zero-order hold (ZOH) or first-order (i.e., linear) interpolator, depending on the $f_R/f_{CKV/N}$ clock rate ratio and the level of the targeted performance. The compensating path, on the other hand, can be as simple as the ZOH, which is mainly due to the low-pass transfer function of the reference phase accumulator. The DCO clock edge divider by N can be easily realized with low power consumption using static CMOS dividers in scaled CMOS technology. The second DCO divider shown in Fig. 3.19 is fractional, and could be implemented according to the topology of Fig. 3.20. Its purpose is to produce a stable symbol-rate $(1/T_s)$ clock or its integer multiple for the purpose of symbol-rate processing and pulse-shape filtering. Note that the modulating data rate in Fig. 3.19 is channel dependent, and also has a second-order dependency on its instantaneous frequency deviation. However, maintaining a harmonic relationship of the modulating clock rate to the DCO resonant frequency is highly beneficial to avoid injection pulling

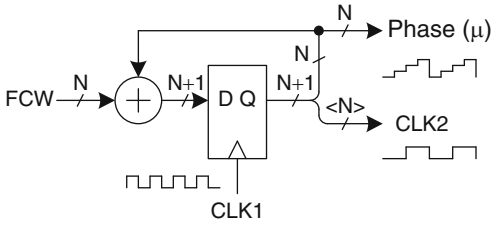

Fig. 3.20 Digital fractional-N edge divider

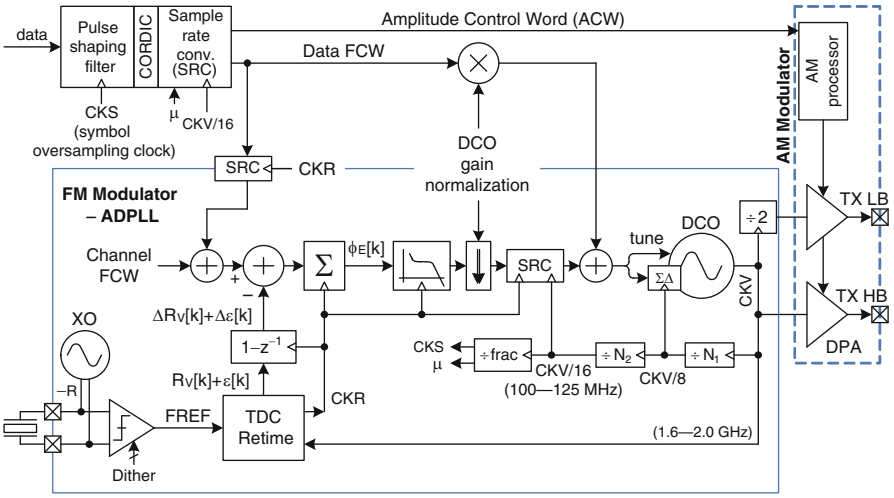

Fig. 3.21 Implementational block diagram of an EDGE polar transmitter based on the multirate DFC with three clock domains: FREF (f_R), CKV (f_V/N) and CKS ($1/T_s$: symbol rate)

spurs [35]. The symbol rate processing in the digital baseband and the pulse-shape filtering, on the other hand, are preferably implemented in the fixed-frequency clock (integer multiple of the symbol rate) that is channel-independent. It implies that the FCW fractional number to the Fig. 3.20 divider must be channel dependent with possible dependency (in case it might be significant) on the instantaneous frequency deviation.

3.6.2.2 Frequency Modulator Within an All-Digital Polar Transmitter

Figure 3.21 demonstrates the use of the above principles of multirate ADPLL-based frequency modulator to realize an all-digital polar transmitter for wireless applications. It is based on the Fig. 3.19 architecture with added details from Fig. 3.20 and Fig. 3.12, as well as the crystal oscillator (XO) with a dither control, the difference-mode phase detector [8], back-end digital transmit modulator and the digital power amplifier (DPA)-based amplitude modulator (AM). The low-band (LB) carrier is obtained by edge-dividing by two the CKV clock of the high-band (HB) carrier. The DPA's for HB and LB are separate.

In addition to the two clock domains in Fig. 3.19, a third symbol oversampling clock (CKS) domain is introduced that is of fixed frequency related to the symbol rate and independent from FREF. The multirate ADPLL architecture features support of modulating samples of much higher rate than the reference clock. In fact, FREF does not play any role in the data modulation. Consequently, the XO could be free-running and the reference frequency adjustment performed through FCW. The CKV/16 clock is used to obtain the channel-independent rate through a fractional clock edge division. It clocks the digital back-end transmit path circuits that perform the I/Q pulse-shape filtering on a clock rate that is an integer multiple of the $1/T_s$ symbol rate. In addition, the CO-ORDInate Calculator (CORDIC) conversion into the ρ and θ polar representation is performed at that rate. An additional sample-rate converter (SRC) circuit converts the symbol-related sampling frequency into the channel-dependent CKV/N rate in order to properly interface with the DCO and DPA. For other standards, whose I/Q bandwidth is much wider than that of EDGE, it might be more beneficial to place the CORDIC after the SRC. CORDIC is an iterative algorithm with internal operations running at 8–16x higher rate. Generating that internal CORDIC clock might be more beneficial if a simple division of the DCO clock were used.

The phase error ϕ_E samples at FREF rate get converted to channel-dependent CKV/16 rate by the sample-rate converter (SRC) and merged with the modulating samples of the same rate. The fractional bits get further dithered by the $\Sigma\Delta$ modulator operating at CKV/8 rate. This way, the injection pulling spurs of the prior implementations [7, 8], with the input at FREF rate, are avoided. The DCO $\Sigma\Delta$ modulator clock is obtained by virtue of $N_1 = 8$ division of the DCO clock. This CKV/8 clock is further divided by two to obtain the CKV/16 clock, which is used by the digital front-end of the FM and AM paths. Referring to Fig. 3.18, the first replica at $f_s =$ CKV/16 rate or 110–125 MHz is beyond the protected receive low band and only needs to meet the relaxed FCC requirements. The CKV/16 clock is also used as the interpolated sampling rate of the phase error corrections.

The single DCO gain-normalization multiplier $f_R/\widehat{K}_{DCO}$ of the prior implementations [7, 8], whose purpose is to normalize the transfer function of the DCO to the reference frequency f_R and thus make it independent from the process, voltage and temperature (PVT) variations, gets split into two parts: a fine precision multiplier in the data modulation path and a coarse multiplier (right bit shift) of the filtered ϕ_E. While the fine DCO transfer function precision (e.g., 0.5–5%, depending on the modulation standard and loop bandwidth) is needed for the distortion-free modulation, only a rough approximation of it (e.g., 5–25%) would be required to establish acceptable range of the closed-loop ADPLL bandwidth. The PLL loop bandwidth affects mainly the settling time and the noise rejection, so its deviation of 5–25% would have minimal effect on the system performance. It should be emphasized that the error in the normalization of the ϕ_E samples is quite benign since it uniformly expands or contracts all the zero and pole locations of the ADPLL closed-loop transfer function.

The split of the $f_R/\widehat{K}_{DCO}$ multiplier is beneficial for several reasons. First, the accurate, hence complex, multiplier is no longer present within the ADPLL loop.

Only a trivial multiplier of short computational delay is needed there. Hence it will not affect the ADPLL loop delay, which could worsen the phase margin in case of a wide bandwidth operation. The accurate multiplier now is only required in the feedforward transmit path, so adding pipelining delay stages should have no consequence on the system performance. Second, the $f_R/\widehat{K}_{DCO}$ multiplier adjustment can now be performed at anytime during the data transmission. This would not be possible in the prior architectures without making hits or perturbations. The ϕ_E samples after the loop filter typically have a large dc component (this is independent of the loop type), so changing the multiplier value will produce an instant change to the DCO tuning word, thus creating sudden frequency deviation steps. The normalization adjustment of the DCO gain during the data modulation could be beneficial for faster settling, but it is necessary in case of a full-duplex operation, which allows no time for off-line adjustments.

3.6.2.3 Phase Detector in the Multirate ADPLL

The ADPLL of Fig. 3.21 operates in the phase domain as follows: The integer part of the variable phase $R_V[k]$ is obtained by sampling, on FREF clock, the current count $R_V[i]$ of the DCO clock edges. The fractional part of the variable phase $\varepsilon[k] = [0,1)$ is obtained from the TDC-based interpolator, whose normalized output $[0,1)$ signifies the position of the FREF edge with respect to the two neighboring DCO edges. The integer and fractional parts are added together to form the fixed-point variable phase $R_V[k] + \varepsilon[k]$. The phase error $\phi_E[k]$ is obtained by subtracting the differentiated variable phase from FCW and integrating the result. The direct calculation of the reference phase $R_R[k]$ is in this case not needed.

This difference form of the phase detection produces almost identical results as the original direct form [7], in which the phase error was directly calculated as $\phi_E[k] = R_R[k] - (R_V[k] + \varepsilon[k])$. The only difference between these two forms is an arbitrary integration constant of the difference form. (Mathematically, integration following the differentiation is a unity operation except for the integration constant C.) This has a consequence of a non-zero phase shift between FREF and CKV even for the type-II ADPLL configuration. However, since the ADPLL typically operates in a non-integer-N configuration, and the absolute phase of the communication path is never relied upon anyway, this effect is immaterial.

The practical benefits, however, are substantial. The differential form of the phase detector allows to "freeze" the time and to stop ramping the phase error, which is found useful during expected external perturbations, such as power amplifier (PA) ramp, a digital baseband (DBB) clock switchover or an external FLASH memory access. Since the phase error is an integral of the frequency error, a generally non-zero frequency error (e.g., during settling) will results in a local ramp of the phase error. Freezing the loop in order to avoid reaction to a transient but known perturbation is non-trivial in case of the direct-form phase detector. However, it only requires zeroing out the input of the final accumulator (i.e., frequency error) in case of the differential-form phase detector. This feature was frequently relied upon during the field operation of the presented architecture.

3.7 Discrete-Time Receiver (DT-RX)

3.7.1 Receiver Architecture

The receiver architecture shown in Fig. 3.22 [20] uses *direct RF sampling* [7,39,40] in the receiver front-end path. In the past, only *subsampling* mixer receiver architectures have been demonstrated: They operate at lower IF frequencies [41,42] and suffer from noise folding and exhibit susceptibility to clock jitter. A recent study [43] uses a high sampling frequency of 480 MHz after the mixer with an RC filtering stage to achieve sufficient programmability and flexibility for SDR receiver, which is presented in Chapter 4. In this architecture, discrete-time analog signal-processing is used to sample the RF input signal at Nyquist rate of the carrier frequency as it is then down-converted, down-sampled, filtered and converted from analog to digital with a discrete-time $\Sigma\Delta$ ADC. This method achieves great selectivity right at the mixer level. The selectivity is digitally controlled by the local oscillator (LO) clock frequency and capacitance ratios, both of which are extremely well controlled and precise in deep-submicron CMOS processes. The discrete-time filtering at each signal-processing stage is followed by successive decimation. The main philosophy in building the receive path is to provide all the filtering required by the standard as early as possible using a structure that is quite amenable to migration to the more advanced deep-submicron processes. This approach significantly relaxes the design requirements for the following baseband amplifiers.

Following the low-noise amplifier (LNA), the signal is converted into current using a transconductance amplifier (TA) stage and down-converted into a programmable low-IF frequency by integrating it on a sampling capacitor. After initial decimation through a sinc filter response, a series of IIR filtering follows RF sampling for close-in interferer rejection. These signal-processing operations are performed in the multi-tap direct sampling mixer (MTDSM) that receives its clocks from the digital control unit (DCU). A $\Sigma\Delta$ ADC containing a front-end gain stage follows. A feedback control unit (FCU) provides a single-bit feedback to the MTDSM to establish the common mode voltage for the MTDSM while canceling out differential offsets. The output of the I/Q ADCs is passed on to digital receive (DRX) chain. The first rate change filter (RCF1) provides anti-aliasing and

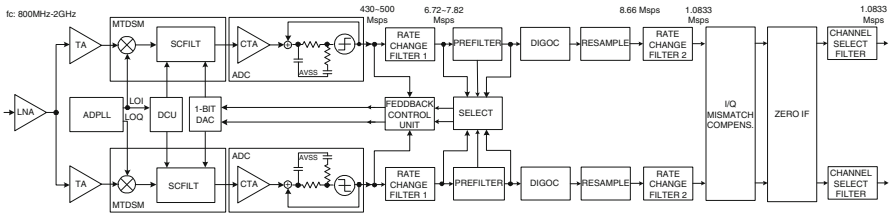

Fig. 3.22 Block diagram of the receiver. (From [36], ©2006 IEEE.)

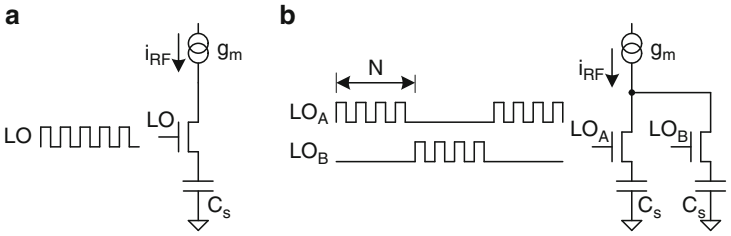

Fig. 3.23 Temporal MA operation at RF rate: (**a**) single-ended, (**b**) pseudo-differential configurations

decimation filtering to reduce the clock rate by 16. Pre-filtering (PREF) is then performed to assist digital resampling (RES) operation. The residual dc offset that could not be corrected by the FCU is corrected by digital offset canceller (DIGOC). The resampler follows and converts the sample rate from LO dependent clock rate to a fixed output rate of 8.66 MS/s. Next, the sample rate is decimated by a second rate change filter to the following I/Q mismatch block. The IF frequency is then converted from the low-IF to dc by the ZERO IF block. The final filtering is performed using a fully programmable 64-tap channel select finite-impulse response (FIR) filter.

One significance of this work is in demonstrating the feasibility of obtaining low noise figure in a receive chain in the presence of more than a million digital gates. Another significance is the development of very low-area, simple and highly programmable analog blocks that are controlled by software to guarantee the best achievable performance. A third significance is the architecture of analog structures that are amenable to migration from one process node to the next without significant rework. Signal processing is used to reduce analog area and complexity. The radio solution was targeted to meet quad-band GSM specification in addition to supporting several experimental modes of operation.

3.7.2 Direct Sampling Mixer

The basic idea of the current-mode direct sampling mixer [7, 39] is illustrated in Fig. 3.23a. The *low-noise transconductance amplifier* (LNTA) converts the received RF voltage v_{RF} into i_{RF} in current domain through the transconductance gain g_m. The current i_{RF} gets switched by the half-cycle of the *local oscillator* (LO) and integrated into the sampling capacitor C_s. Since it is difficult to switch the current at RF rate, it could be merely redirected to an identical sampler that is operating on the opposite half-cycle of the LO clock, as shown in Fig. 3.23b for a pseudo-differential configuration.

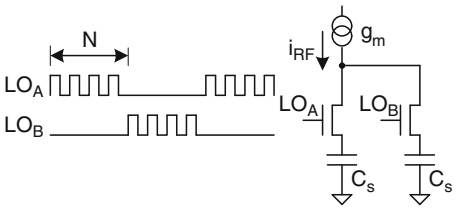

Fig. 3.24 Temporal MA operation at RF rate with cyclic charge readout. (From [37], ©2005 IEEE.)

If the LO oscillating at f_0 frequency is synchronous and in phase with the sinusoidal RF waveform, the voltage gain of a single RF half-cycle is

$$G_{v,RF} = \frac{1}{\pi} \cdot \frac{1}{f_0} \cdot \frac{g_m}{C_s} \tag{3.1}$$

and the accumulated charge on the sampling capacitor is

$$G_{q,RF} = \frac{1}{\pi} \cdot \frac{1}{f_0} \cdot g_m \tag{3.2}$$

In the above equations, the $\frac{1}{\pi}$ factor is contributed by the half-cycle sinusoidal integration. As an example, if $g_m = 30$ mS, $C_s = 15.925$ pF and $f_0 = 2.4$ GHz, then $G_{v,RF} = 0.25$.

3.7.3 Temporal Moving-Average

Continuously accumulating the charge as shown in Fig. 3.23 is not very practical if it cannot be read out. In addition, a mechanism to prevent the charge overflow is needed. Both of these operations are accomplished by fixing the integration window length followed by charge readout phase that will also discharge the sampling capacitor such that the next period of integration would start from the same zero condition. The RF sampling and readout operations are cyclically rotated on both C_s capacitors as shown in Fig. 3.24. When LO_A rectifies N RF cycles that are being integrated on the first sampling capacitor, LO_B is off and the second sampling capacitor charge is being read out. On the next N RF cycles the operation is reversed. This way, the charge integration and readout occur at the same time and no RF cycles are missed.

The sampling capacitor integrates the half-rectified RF current over N cycles. The charge accumulated on the sampling capacitor and the resulting voltage ($V = Q/C_s$) increases with the integration window, thus giving rise to a discrete signal-processing gain of N.

The temporal integration of N half-rectified RF samples performs an FIR operation with N all-one coefficients, also known as *moving-average* (MA), according to the following equation:

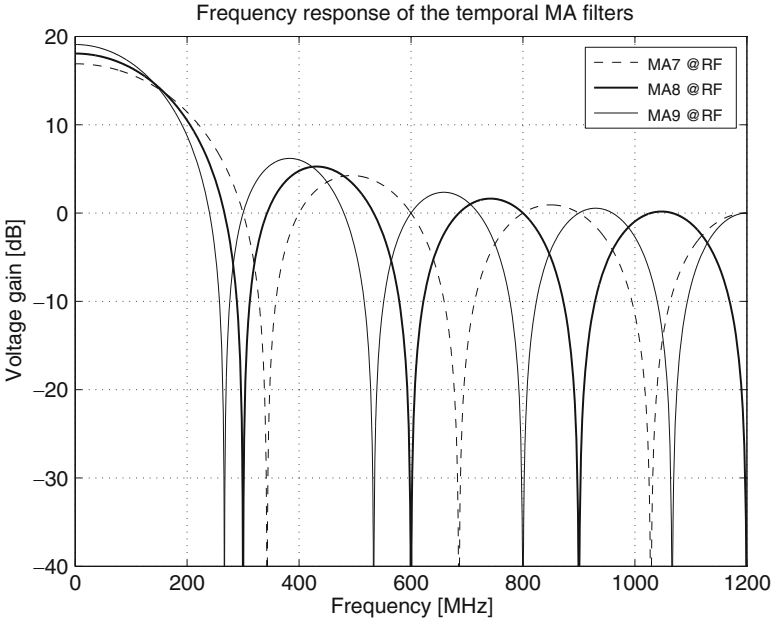

Fig. 3.25 Transfer function of the temporal MA operation at RF rate. (From [37], ©2005 IEEE.)

$$w_i = \sum_{l=0}^{N-1} u_{i-l} \tag{3.3}$$

where u_i is the ith RF sample of the input charge sample, and w_i is the accumulated charge. Since the charge accumulation is performed on the same capacitor, this formula could also be used in the voltage domain. Its frequency response is a *sinc* function and is shown in Fig. 3.25 for $N = 8$ (solid line) and $N = 7,9$ (dotted lines) with sampling rate $f_0 = 2.4\,\text{GHz}$. It should be noted that this filtering is performed on the same capacitor but in the time domain, resulting in a most *faithful* reproduction of the transfer function.

Because the MA output is read out at the lower rate of N RF clock cycles, there is an additional aliasing with foldover frequency at $f_0/2N$ and located halfway to the first notch. Consequently, the frequency response of MA = 7 with decimation of 7 exhibits less aliasing and features wider notches than MA = 8 or MA = 9 with decimation of 8 or 9, respectively.

It should be emphasized that the voltage G_v and charge G_q signal-processing gains of the temporal moving-average (TMA) (followed by decimation) are merely due to the sampling time interval expansion of this discrete-time system (the sampling rate of the input is at the RF frequency): $G_{v,tma} = G_{q,tma} = N$.

In the following analysis, the RF half-cycle integration voltage gain of $\frac{g_m}{\pi C_s f_0}$ is tracked separately. Since this gain depends on the absolute physical parameters

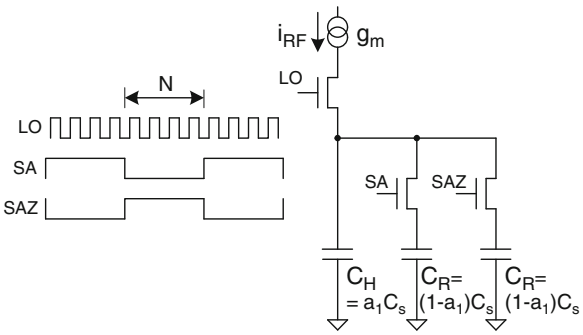

Fig. 3.26 IIR operation with cyclic charge readout. (From [37], ©2005 IEEE.)

of usually low tolerance (g_m value of the preceding LNTA stage and the total integrating capacitance of the sampling mixer), it is advantageous to keep it decoupled from the discrete signal-processing gain of the MTDSM.

3.7.4 High-Rate IIR Filtering

Figure 3.24 is now modified to include recursive operation that gives rise to the IIR filtering capability, which is generally considered stronger than that of FIR.

A "history" sampling capacitor C_H is added in Fig. 3.26. The integration is continually performed on the "history" capacitor $C_H = a_1 C_s$ and one of the two rotating "charge-and-readout" capacitors $C_R = (1 - a_1)C_s$ such that the total RF integrating capacitance, as seen by the LNTA, is always $C_H + C_R = C_s$. When one of the C_R capacitors is being used for readout, the other is being used for RF integration.

The IIR filtering capability comes into play in the following way: The RF current is integrated over N RF cycles, as described before. This time, the charge is shared on both C_H and C_R capacitors proportionately to their capacitance values. At the end of the accumulation cycle, the active C_R capacitor, that stores $(1 - a_1)$ of the total charge, stops further accumulation in preparation for charge readout. The other rotating capacitor joins the C_H capacitor in the RF sampling process and, at the same time, obtains $\frac{1-a_1}{a_1+(1-a_1)} = 1 - a_1$ of the total remaining charge in the "history" capacitor, provided it has no initial charge at the time of commutation. Thus the system retains a_1 portion of the total system charge of the previous cycle.

If the input charge accumulated over the most-recent N RF samples is w_j then the charge s_j stored in the system at sampling time j, where $i = N \cdot j$, (as stated earlier, i is the RF cycle index) could be described as a single-pole recursive IIR equation:

$$s_j = a_1 s_{j-1} + w_j \tag{3.4}$$

$$x_j = (1 - a_1)s_{j-1} \tag{3.5}$$

$$a_1 = \frac{C_H}{C_H + C_R} \tag{3.6}$$

The output charge x_j is $(1-a_1)$ of the system charge in the most-recent cycle. This discrete-time IIR filter operates at f_0/N sampling rate and introduces a single pole with the frequency attenuation of 20 dB/dec. The equivalent pole location in the continuous-time domain for $f_{c1} \ll f_0/N$ is

$$f_{c1} = \frac{1}{2\pi}\frac{f_0}{N} \cdot (1-a_1) = \frac{1}{2\pi}\frac{f_0}{N} \cdot \frac{C_R}{C_H + C_R} \tag{3.7}$$

Since there is no sampling time expansion for the IIR operation, the discrete signal-processing charge gain is 1. In other words, because of the charge conservation principle, the input charge per sample interval is on average the same as the output charge. For the voltage gain, however, there is an impedance transformation of $C_{input} = C_s$ and $C_{output} = (1-a_1)C_s$, thus resulting in a gain.

$$G_{q,iir1} = 1 \tag{3.8}$$

$$G_{v,iir1} = \frac{1}{1-a_1} = \frac{C_H + C_R}{C_R} \tag{3.9}$$

As an example, the IIR filtering with a single coefficient of $a_1 = 0.9686$, placing the pole at $f_{c1} = 1.5\,\text{MHz}$, ($C_R = 0.5$ pF, $C_H = 15.425$ pf) is performed at $f_0/N = 2.4\,\text{GHz} / 8 = 300\,\text{MHz}$ sampling rate and it follows the FIR MA=8 filtering of the input at f_0 RF sampling rate. The voltage gain of the high-rate IIR filter is 31.85 (30.06 dB).

3.7.5 Additional Spatial MA Filtering Zeros

For practical reasons, it is difficult to read out the x_j output charge of Fig. 3.26 at $f_0/N = 300\,\text{MHz}$ rate. The output charge readout time is extended $M = 4$ times by adding redundancy of four to each of the two original C_R capacitors as shown in Fig. 3.27. The input charge is cyclically integrated within the group of four C_R capacitors. Adding the redundant capacitors gives rise to an additional anti-aliasing filtering just before the second decimation of M. This could also be considered as equivalent to adding additional $M-1$ zeros to the IIR transfer function in (3.4). After the first bank of four capacitors gets charged ($S_{A1} - S_{A4}$ in Fig. 3.27), the second bank ($S_{B1} - S_{B4}$) is in the process of being charged and the charge on the first bank of capacitors is summed and read out (R_1). By physically connecting together the four capacitors, an FIR filtering is performed, which is described as the spatial moving-average (SMA) of $M = 4$:

$$y_k = \sum_{l=0}^{M-1} x_{k-l} \tag{3.10}$$

where, y_k is the output charge and sampling time index $j = M \cdot k$. R_A and R_B in Fig. 3.27 are the readout/reset cycles during which the output charge on the four

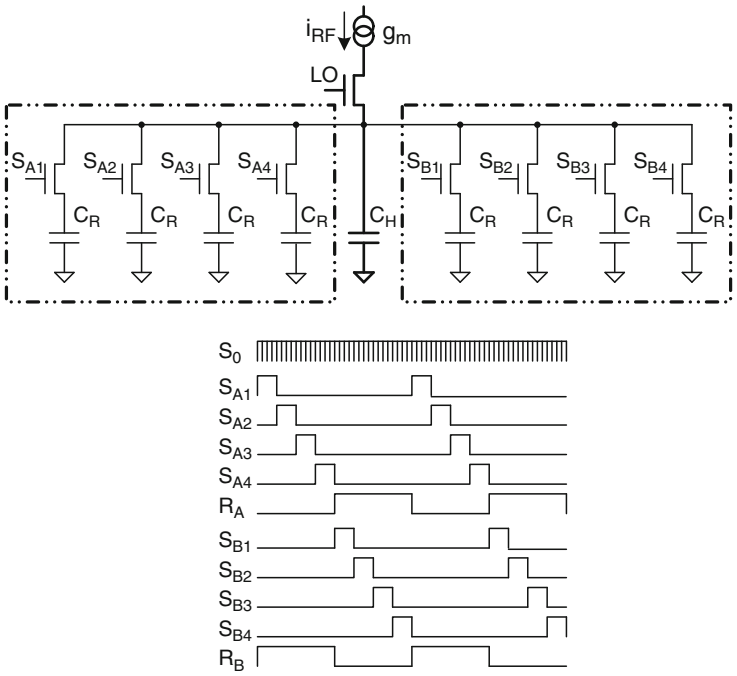

Fig. 3.27 IIR operation with additional FIR filtering. The readout and reset circuitry is not shown. (From [37], ©2005 IEEE.)

non-sampling capacitors is transferred out and the remnant charge is reset before the capacitors are put back into the sampling operation. It should be noted that after the reset phase, but before the sampling phase, the capacitors are unobtrusively precharged [40] to implement a dc-offset cancellation or to accomplish a feedback summation for the $\Sigma\Delta$ loop operation.

Since the charge of four capacitors is added, there is a charge gain of $M = 4$ and a voltage gain of 1. Again, as explained before, the charge gain is due to the sampling interval expansion: $G_{q,sma} = M$ and $G_{v,sma} = 1$.

Figure 3.28 shows frequency response of the TMA with a decimation of 8 ($G_v = 18.06$ dB), the IIR filter operating at RF/8 rate ($G_v = 30.06$ dB) and the spatial MA filter operating at RF/32 rate ($G_v = 0$ dB) with a decimation of 4. The solid line is the composite transfer function with the dc gain of $G_v = 48.12$ dB. The first decimation of $N = 8$ reveals itself as aliasing. It should be noted that it is possible to avoid aliasing of a very strong interferer into the critical IF band by simply changing the decimation ratio N. This brings out advantages of integrating RF/analog with digital circuitry by opening new avenues of novel signal-processing solutions not possible before.

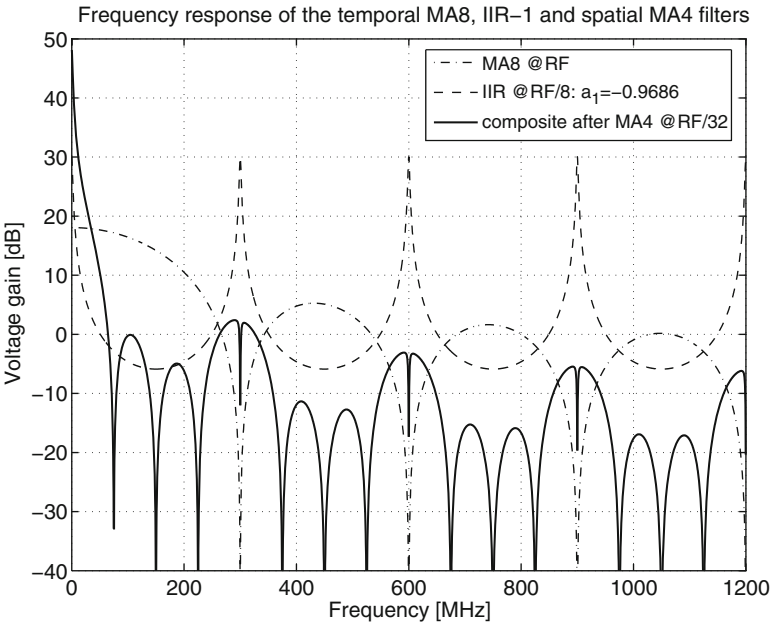

Fig. 3.28 Transfer function of the temporal MA filter and the IIR filter operating at RF/8 rate. The solid line is the composite transfer at the output of the spatial MA filter. (From [37], ©2005 IEEE.)

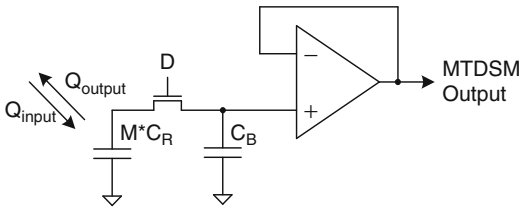

Fig. 3.29 Second IIR filter. (From [37], ©2005 IEEE.)

3.7.6 Lower-Rate IIR Filtering

The voltage stored on the rotating capacitors cannot be readily presented to the MTDSM block output without an active buffer that would isolate the high impedance of the mixer from the required low driving impedance of the output. Figure 3.29 shows the mechanism to realize the second, lower-rate, IIR filtering through passive charge sharing. The active element, the operational amplifier, does not actually take part in the IIR filtering process. It is merely used to sense voltage of the buffer feedback capacitor C_B and present it to the output with a low driving impedance. Figure 3.29 additionally suggests possibility of differentially combining, through the operational amplifier, the opposite (180° apart) processing path.

The charge y_k accumulated on the $M = 4$ rotating capacitors is shared during the dumping phase with the buffer feedback capacitor C_B. At the end of the dumping phase, the $M \cdot C_R$ capacitors get disconnected from the second IIR filter and their charge reset before they could be re-engaged in the MTDSM operation of Fig. 3.27. This charge loss mechanism gives rise to IIR filtering. If the input charge is y_k, then the charge z_k stored in the buffer capacitor C_B at sampling time k is

$$z_k = a_2(z_{k-1} + y_k) = a_2 z_{k-1} + a_2 y_k \tag{3.11}$$

$$a_2 = \frac{C_B}{C_B + MC_R} \tag{3.12}$$

Equation (3.11) describes a single-pole IIR filter with coefficient a_2 and input y_k scaled by a_2, where a_2 corresponds to the storage-to-total capacitance ratio $\frac{C_B}{C_B+MC_R}$. Conversely, due to the linearity property, it could also be thought of as an IIR filter with input y_k and output scaled by a_2.

This discrete-time IIR filter operates at f_0/NM sampling rate and introduces a single pole with the frequency transfer function attenuation of 20 dB/dec. The equivalent pole location in the continuous-time domain for $f_{c2} \ll f_0/(NM)$ is

$$f_{c2} = \frac{1}{2\pi}\frac{f_0}{NM} \cdot (1 - a_2) = \frac{1}{2\pi}\frac{f_0}{NM} \cdot \frac{MC_R}{C_B + MC_R} \tag{3.13}$$

The actual MTDSM output is the voltage sensed on the buffer feedback capacitor z_k/C_B. The previously used charge stream model cannot be directly applied here because the "output" charge z_k is not the one that leaves the system.

The charge "lost" or reflected back into the $M \cdot C_R$ capacitor for subsequent reset is $(1 - a_2)(z_{k-1} + y_k)$. On the basis of the charge conservation principle, the time-averaged values of charge input, y_k, and charge leaked out, $(1 - a_2)(z_{k-1} + y_k)$, should be equal. As stated before, the leak-out charge is not the output from the signal processing standpoint. It should be noted that the amplifier does not contribute to the net charge change of the system and, consequently, the only path of the charge loss is through the same $M \cdot C_R$ capacitors that are reset after the dumping phase.

The output charge z_k stops at the IIR-2 stage and does not further propagate, therefore it is of less importance for signal-processing analysis. The charge discrete signal-processing gain of the second IIR stage is

$$G_{q,iir2} = \frac{a_2}{1 - a_2} = \frac{C_B}{MC_R} \tag{3.14}$$

The input/output impedance transformation is $\frac{MC_R}{C_B}$. Consequently, the voltage gain of IIR-2 is unity.

$$G_{v,iir2} = 1 \tag{3.15}$$

3.7.7 Cascaded MTDSM Filtering

The cascaded discrete signal-processing gain equations of the MTDSM mixer are [38]:

$$G_{q,dsp} = G_{q,tma} \cdot G_{q,iir1} \cdot G_{q,sma} \cdot G_{q,iir2} \tag{3.16}$$

$$= N \cdot 1 \cdot M \cdot \frac{C_B}{MC_R} \tag{3.17}$$

$$= \frac{NC_B}{C_R} \tag{3.18}$$

$$G_{v,dsp} = G_{v,tma} \cdot G_{v,iir1} \cdot G_{v,sma} \cdot G_{v,iir2} \tag{3.19}$$

$$= N \cdot \frac{C_H + C_R}{C_R} \cdot 1 \cdot 1 \tag{3.20}$$

$$= \frac{N(C_H + C_R)}{C_R} \tag{3.21}$$

Including the RF half-cycle integration ((3.1) and (3.2)) the total single-ended gain is:

$$G_{q,tot} = G_{q,RF} \cdot G_{q,dsp} \tag{3.22}$$

$$= \frac{1}{\pi} \cdot \frac{1}{f_0/N} \cdot g_m \tag{3.23}$$

$$G_{v,tot} = G_{v,RF} \cdot G_{v,dsp} \tag{3.24}$$

$$= \frac{1}{\pi} \cdot \frac{1}{f_0/N} \cdot \frac{g_m}{C_R} \tag{3.25}$$

Note the similarity between (3.25) and (3.1). In both cases, the term $R_{sc} = \frac{1}{f_s C_s}$ is an equivalent resistance of a switched-capacitor C_s sampling at rate f_s. For example, if $f_s = 300\,\text{MHz}$ and $C_R = 0.5$ pF, then the equivalent resistance is $R_{sc} = 6.7\ \text{k}\Omega$. Since the MTDSM output is differential, the gain values in the above equations are actually doubled.

The dc-frequency gain $G_{v,tot}$ in (3.25) requires further elaboration. The gain depends only on the g_m of the LNTA stage, rotating capacitor value and the rotation frequency. Amazingly, it does not depend on the other capacitor values, which contribute only to the filtering transfer function at higher frequencies.

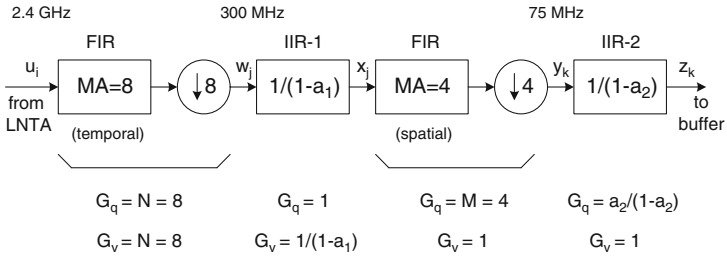

Fig. 3.30 Discrete signal processing in the MTDSM

3.7.8 Near-Frequency Interferer Attenuation

Most of the lower-frequency filtering could be realistically done only with the first and second IIR filters. The two FIR filters do not have appreciable filtering capability at low frequencies and are mainly used for anti-aliasing.

It should be noted that the best filtering could be accomplished by making 3-dB corner frequency of both IIR filters the same and placing them as close to the higher end of signal band as possible.

$$f_{c1} = f_{c2} \tag{3.26}$$

This gives the following constraint:

$$C_B = C_H - (M-1)C_R \tag{3.27}$$

3.7.9 Signal Processing Example

Figure 3.30 shows the block diagram from the signal processing standpoint for our specific implementation of $f_0 = 2.4\,\text{GHz}$, $N = 8$, $M = 4$. The following equations describe the time-domain signal processing: (3.3) for w_j, (3.4) and (3.5) for x_j, (3.10) for y_k, and (3.11) for z_k.

The first aliasing frequency (at $f_0/N = 300\,\text{MHz}$) is partially protected by the first notch of the temporal MA=8 filter. However, for higher-order aliasing and overall system robustness, it has to be protected with a truly continuous-time filter, such as an antenna filter. A typical low-cost Bluetooth-band duplexer can attenuate up to 40 dB at 300 MHz offset.

For the above system with an aggressive cut-off frequency of $f_{c1} = f_{c2} = 1.5\,\text{MHz}$, using $C_R = 0.5$ pF will result in a dc-frequency voltage gain of 63.66 or 36 dB (3.25) and the required capacitance is $C_H = 15.425$ pF (3.7) and $C_B = 13.925$ pF (3.13). The z-domain coefficients of the IIR filters are $a_1 = 0.9686$ and $a_2 = 0.8744$. The dc-frequency gains are $G_{v,iir1} = 31.85$ and $G_{v,iir2} = 1$. The transfer function of these IIR filters is shown in Fig. 3.31. The spatial MA=4, which follows

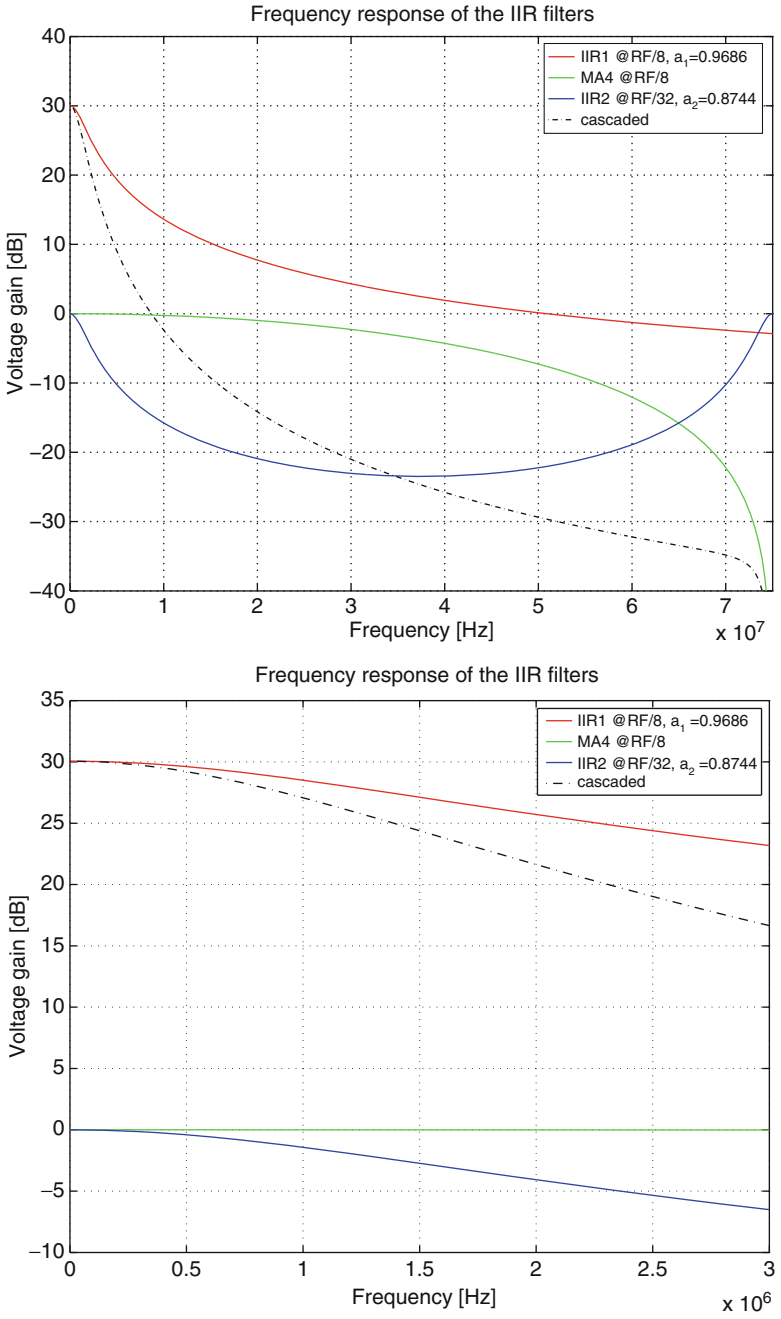

Fig. 3.31 Transfer function of the IIR filters with two poles at 1.5 MHz (bottom zoomed)

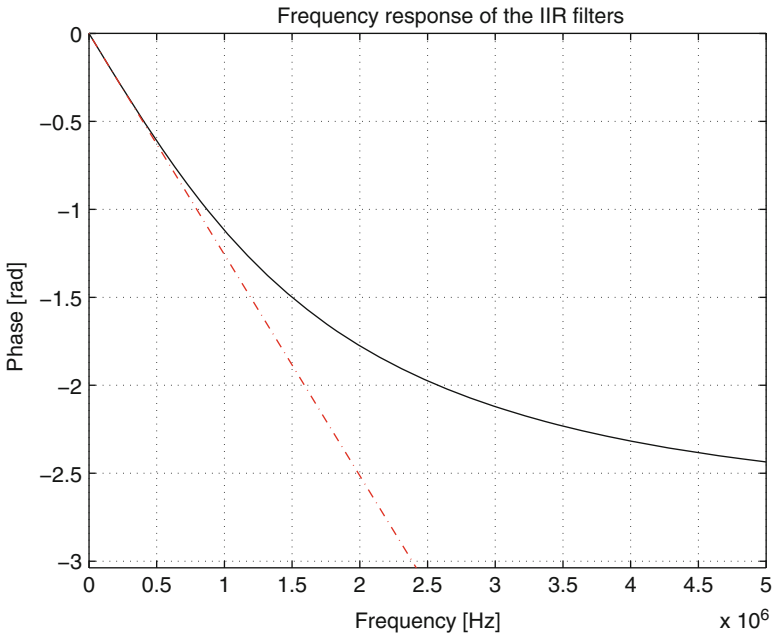

Fig. 3.32 Phase response the IIR filters with two poles at 1.5 MHz

IIR-1, does not appreciably contribute to filtering at lower frequencies but serves as an anti-aliasing filter for the lower-rate IIR-2. Since the 3-dB point of IIR-2 is slightly corrupted by the discrete-time approximation, the composite attenuation at the cut-off frequencies $f_{c1} = f_{c2} = 1.5$ MHz is about 5.5 dB. The attenuation drops to 13 dB at 3 MHz.

Within the 1 MHz band of interest, there is a 3 dB signal attenuation. For the most optimal detector operation, this in-band filtering should be taken into consideration in the matched-filter design. Figure 3.32 shows the phase response of the above structure versus the ideal constant group delay.

3.7.10 MTDSM Feedback Path

The MTDSM feedback correction could be unobtrusively injected into either group of the four rotating capacitors of Fig. 3.27 when they are not in the active sampling state. This way, the main signal path is not perturbed. The feedback correction is accomplished through charge injection/equalization between the "feedback capacitor" C_F and the rotating capacitors C_R in the MTDSM structure by shorting all of them together after the C_R group of capacitors gets reset, but before they are put back to the sampling system. The feedback charge accumulation structure is

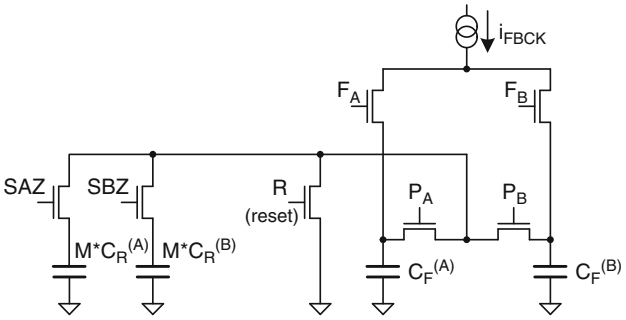

Fig. 3.33 Feedback into the rotating capacitors

shown in Fig. 3.33. Each feedback capacitor C_F is associated with one of the two rotating capacitors of group "A" and "B". These two groups commutate the charging process.

Voltage on the feedback capacitor can be calculated as follows. Charging the feedback capacitor C_F with the current i_{fbck} for the duration of T will result in incremental accumulation of $\Delta Q_{in} = i_{fbck} \cdot T$ charge. This charge gets added to the total charge $Q_F(k)$ of the feedback capacitor at the kth time instance.

$$Q_F(k) = Q_F(k-1) + \Delta Q_{in} = Q_F(k-1) + i_{fbck} \cdot T \tag{3.28}$$

During the charge distribution moment, the feedback capacitor gets connected with the previously-reset group of rotating capacitors $M \cdot C_R$. The charge depleted from C_F is dependent on the relative capacitor values.

$$\Delta Q_{out}(k) = \frac{MC_R}{C_F + MC_R} Q_F(k) \tag{3.29}$$

The charge transferred to the rotating capacitors is proportional to the total accumulated charge Q_F or voltage on the feedback capacitor $V_F = Q_F/C_F$. At first, the accumulated charge is small, so the outgoing charge is small. Since the incoming charge is constant, the Q_F charge will continue accumulation until the net charge intake becomes zero. Equilibrium is reached when $\Delta Q_{in}(k) = \Delta Q_{out}(k)$.

$$i_{fbck} \cdot T = \frac{MC_R}{C_F + MC_R} Q_F(k) \tag{3.30}$$

Transformation of the above gives the equilibrium voltage.

$$V_{F,eq} = i_{fbck} \cdot T \cdot \frac{C_F + MC_R}{C_F \cdot MC_R} \tag{3.31}$$

The $\Delta Q_{out,eq}$ charge transfer into the rotating capacitors at equilibrium will create voltage on the bank of rotating capacitors.

$$V_R = \frac{i_{fbck} \cdot T}{MC_R} \tag{3.32}$$

As shown in Sect. 3.7.6, the voltage transfer function from the rotating capacitors to the history capacitor is unity. Therefore, the bias voltage developed on C_H is

$$V_H = \frac{i_{fbck} \cdot T}{MC_R} \tag{3.33}$$

3.8 RF Built-In Self-Test (RF-BIST)

The testability issues of an RF circuit are probably last on the RF circuit designer's mind. However, a considerable portion of the overall RF-SoC fabrication cost is in its testing. The testing costs are high in case of a complex mixed-signal SoC for RF wireless applications involving extensive and time-consuming defect, performance, and standard compliance measurements. These factory measurements are traditionally made using expensive and sophisticated test equipment. Furthermore, due to the complexity of the equipment and test settings, these measurements cannot be executed at-probe on wafer, before the IC chip is packaged, nor in the field after the chip leaves the factory environment. Consequently, it is desirable to improve testing costs and coverage during the complete life-cycle of an SoC in order to maximize wafer yield, profitability, and customer satisfaction.

Frequency synthesizers and transmitters are conventionally tested for RF performance and wireless standard compliance by measuring their output RF port for the correct carrier frequency, phase noise spectrum, integrated phase noise, spurious content, modulated spectrum, and modulated phase error trajectory (see [22] for GSM) while stimuli and control signals are applied. The RF-BIST measurement method performs signal-processing calculations on a lower-frequency internal signal to ascertain the RF performance without external test equipment. This significantly saves test time and costs, and increases coverage.

Several RF-BIST functions are now feasible with the all-digital transmitter and digitally-intensive discrete-time receiver. They include digital loop-back, mixed-signal feedback loop (for dc offset cancellation) and TX-RX RF loop-back at the mixer. Coupling at the package can be used to realize an external TX-RX feedback loop that incorporates the entire transceiver. A programmable sine/cosine waveform generates feedback signals that are fed to the mixer through the offset correction loop to establish an additional analog feedback. This loop can be used to perform several calibration and test functions. Because of reuse of the on-die processor, very little hardware overhead is required for RF-BIST.

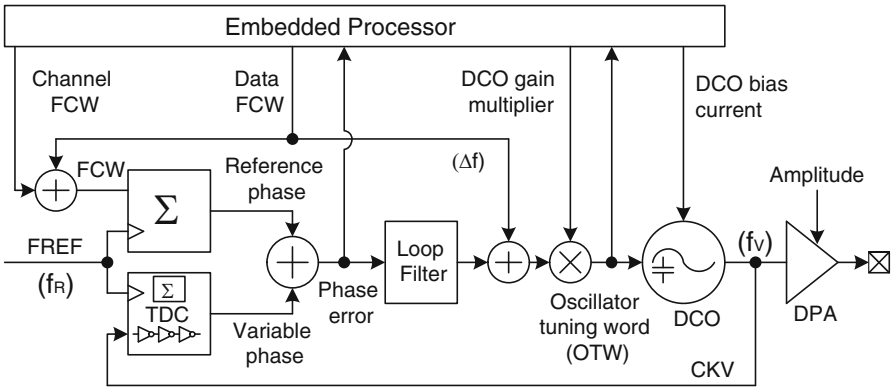

Fig. 3.34 An embedded processor providing digital assistance to the ADPLL-based transmitter. DPA is a digitally-controlled amplifier

Despite the "all-digital" classification of the Fig. 3.7b ADPLL, i.e., all major blocks having exclusively digital inputs and outputs, the internal nature of the DCO and TDC is still analog. Consequently, in order to maintain the precise transfer function characteristic, the process, voltage and temperature (PVT)-dependent conversion gain of these blocks needs to be tracked and compensated. Figure 3.34 includes the relevant DCO interface details. Also shown is a tightly-coupled embedded RISC processor [23] that provides various types of digital assistance.

The output of the filtered phase error is multiplied by a DCO gain normalization factor K_{DCO} such that the gain from the FCW fixed-point data feed to the RF output is independent from the PVT and is exactly f_R/LSB. This ensures that the ADPLL loop bandwidth is known accurately and the modulation transfer function is flat from dc to half of the sampling frequency. The embedded processor is used to accomplish this normalization using an on-line LMS algorithm described in [21].

The embedded processor is also used to reduce the overall current consumption while maximizing the RF performance [23]. The parameter of interest to which the DCO current and voltage need to be adjusted is the overall close-in RF transmitter performance captured in such metrics as the modulation spectrum, as well as rms and peak of the phase trajectory error (PTE), in case of GSM. These measurements are fairly complicated and require the use of an expensive external test equipment connected to the RF TX output port. At best, they can be used in factory to calibrate for the process changes but they simply rule out compensation for environmental conditions. The novel approach proposed in [19] solves the problem by calculating statistics of an internal signal, i.e., digital phase error samples of Fig. 3.34, as a proxy for the performance at the RF output port. In this method, the FFT, rms and peak of the digital phase error samples are processed by the internal processor in real-time to estimate the phase noise spectrum, and rms and peak of the PTE, respectively, at the RF output. The calculated statistics are then compared directly against the GSM specifications. Figure 3.35 shows such comparison. This allows to trade off

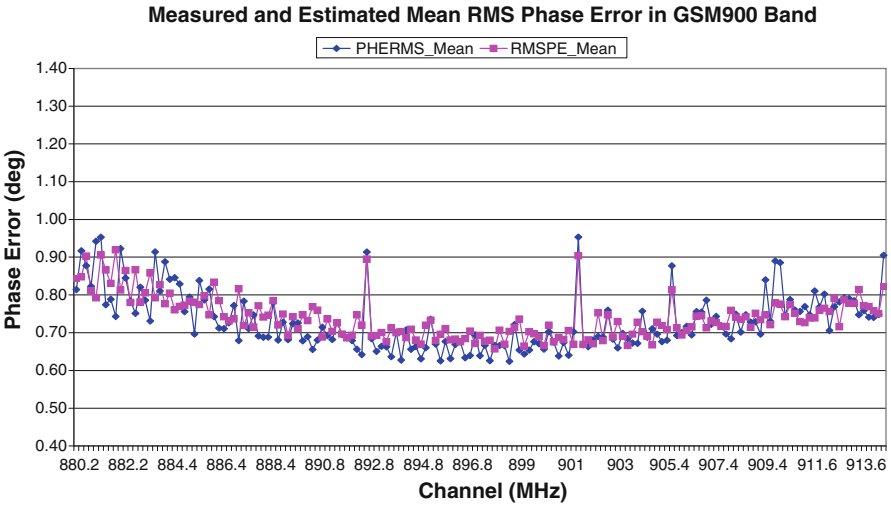

Fig. 3.35 Measured modulation distortion (i.e., phase trajectory error) vs. calculated from the digital phase error statistics (i.e., rms of PHE)

supply voltage and current consumption versus the required circuit performance. For example, the max. DCO bias current of 18 mA in [12] can be reduced to as low as 6 mA if the wafer process is not weak and the die temperature is not high. Figure 3.36 shows the tradeoff between the measured phase noise performance and the current consumption.

3.9 Conclusion

We have presented the recent revolution in the area of RF circuit design in highly-scaled CMOS processes. It was driven by the desire to exploit the increasing power and affordability of CMOS technology for the purpose of reducing the wireless solution costs through system-on-chip (SoC) integration. It was found that implementing the traditional RF circuits in more and more advanced CMOS would make its performance increasingly worse, so the new RF architectures and design approaches had to be invented. Enter "Digital RF": The transformation of the RF transceiver functionality into the novel time-domain operation, as embodied by the time-to-digital converter (TDC)- and digitally-controlled oscillator (DCO)-based all-digital phase-locked loop (ADPLL), and the discrete-time receiver exploiting sophisticated signal processing, such as IIR. Enter "Digital assistance of RF": heavy use of digital logic and memory to assist with the linear performance of analog transistors – it also falls under the umbrella of this new technology. The new approach has proven to be very successful in the commercial world by substantially

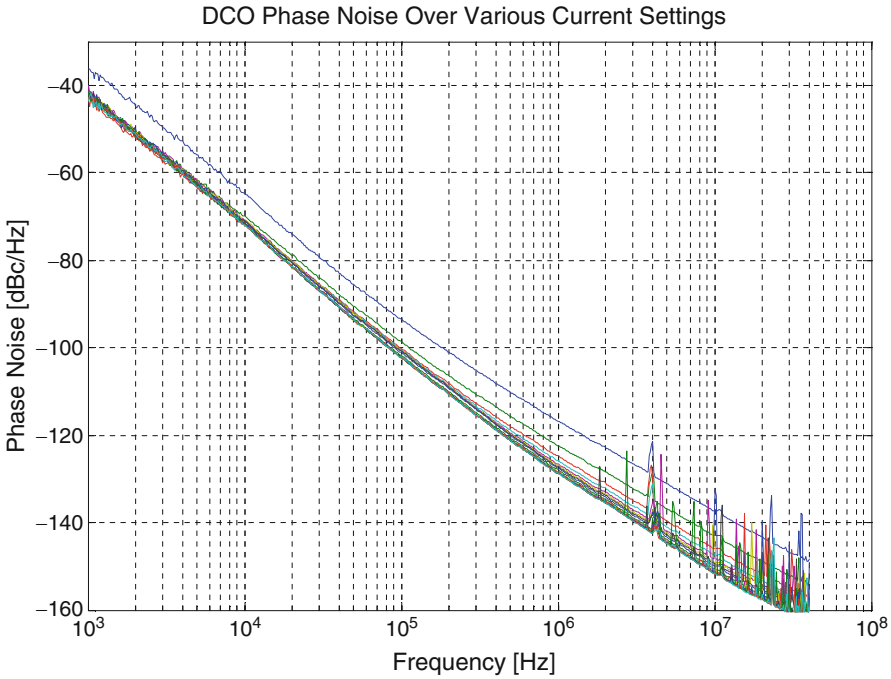

Fig. 3.36 Measured DCO phase noise over various bias current settings. Higher code setting results in a better phase noise but the improvement vanishes at the highest code levels

reducing cost, form factor and current consumption while increasing production yield and time-to-market. It is estimated that it powers nowadays about 1/3 of the world's cellular phones and this number is expected to grow given many newly issued patents and patent publications from various companies around the world.

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Chapter 4
Software-Defined Radio Receiver Architecture and RF-Analog Front-End Circuits

Rahim Bagheri, Ahmad Mirzaei, Saeed Chehrazi, and Asad A. Abidi

4.1 Introduction

Wireless bands and services are proliferating across the world. Every six months approximately, a new use for wireless appears, often leading to a new standard. Manufacturers of mobile handsets have a hard time keeping up, because the end user wants to access an increasing number of services from a single handset, and have it adapt to global roaming. In the face of this proliferation a universal software-defined radio (SDR) which can communicate over all bands and standards is in high demand. This chapter covers SDR receievrs (SDR-RX). First an overview of prior SDR receiver (SDR-RX) developments is presented. Then a novel architecture for low power SDR-RX, partly evolved from prior SDR works, is described. A CMOS prototype implementation which covers the 0.5 to 6 GHz spectrum and can tune to a wide range of narrowband and wideband modulations is presented. Main circuit blocks of this SDR-RX including the programmable anti-aliasing analog filter, wideband LNA and high linearity harmonic-rejection mixer are presented. Finally the areas where further performance improvement is needed are highlighted. Due to

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high flexibility and close similarity to the tried and true narrowband receivers, it is foreseeable that this architecture can yield itself to be widely used in future low power SDR-RX products.

4.2 Software-Defined Radio Receiver History

SDR technology has been sought after for long time, but it was Mitola's research in mid-1990s [1] which brought the subject to the attention of the wider range of engineers. Since then, considerable progress has been made on the digital front-end, digital baseband (modem), protocols and the networking layers sections [2–9]. However the radio front-end and particularly the handheld equipment side has made less progress because of the many challenges involved. Essentially RF and analog blocks are almost always custom designed and have the least degree of flexibility. This section summarizes a historical review of previous SDR-RX front-end works, with particular focus on those which culminated our UCLA SDR-RX [10].

4.2.1 Mitola's Architecture

The classic view of an SDR is based on what Mitola envisioned in 1995 [1], where the radio is purely implemented in digital signal processing domain (DSP) except for its data converter blocks (Fig. 4.1). This heavily digitized radio concept provides the highest degree of reconfigurability. It can transmit and receive many channels concurrently, and it has been attractive for cellular base-stations, enabling them to support multi-carrier waveforms.

However, the only practical implementation of Mitola-based SDR is found in UK DERA HF radio [11], covering only the 3-to 30-MHz band, where many military communications take place. In this radio, the HF antenna is followed by a 30-MHz lowpass filter to limit the input signal total dynamic range (Fig. 4.2a), but here we highlight the filter's more fundamental role as the anti-aliasing filter prior to sampling in the analog-to-digital converter (ADC).

With this filter, any blocker above 37.5 MHz is completely suppressed before it aliases in the first Nyquist band of the 75MHz sampling ADC. After the entire HF-band is digitized by a 12-bit 75-MHz A/D converter, the digital front-end down-converts the channel of interest to zero-IF (intermediate frequency), performs the channel select filtering and decimates the initial high sample rate (75 MHz) down to

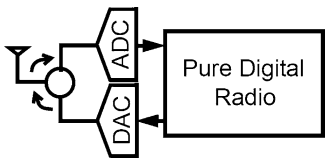


Fig. 4.1 Mitola's SDR hardware concept

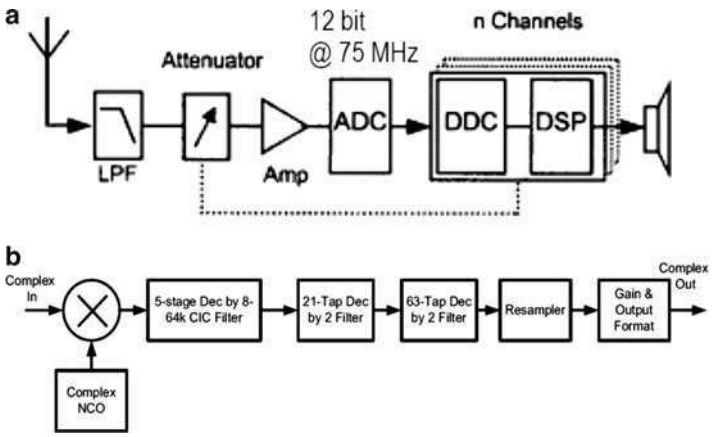


Fig. 4.2 (**a**) UK DERA HF receiver [11] based on Mitolla' SDR hardware view. (**b**) Digital Front-End of UK DERA HF receiver. Extensive use of the cascaded integrator comb (CIC) fiters for downsampling of the zero-IF signal is highlighted

the symbol rate of that channel (Fig. 4.2b). It is educative to note that this work uses cascaded integrator comb (CIC) filters. CIC filters are usually the primary choice for decimation filtering, because their sinc(f)-shaped response nulls all the aliasing components. Even though this HF SDR-RX offers full advantages of an ideal SDR-RX as suggested by Mitola, its frequency coverage is at most limited to half of the maximum sample rate of the ADC –in this case, about 30 MHz. To better understand the consequences of this limitation, let's consider that the carrier frequencies as high as 6 GHz and protocols such as GSM have to be covered (in a typical civilian use SDR-RX). In such case a 12-GHz sample rate ADC with input dynamic range of about 100 to 110 dB for a 200-KHz signal bandwidth is required [12].

Using the following equation this translates to about 12 Nyquist rate bits:

$$\text{ADC Dynamic Range} = 6.02b + 1.76 + 10log10(f_s/2BW) \tag{4.1}$$

where b is the number of bits, f_s is the sample rate, and BW is the desired channel bandwidth. Given today's state of the art and the resolution progress rate of 1.5-bits/6-years as predicted in [13], such ADC is not feasible in near future. Furthermore, following the guidelines set in [13] it is estimated that power consumption of such ADC could be about 500 W. This is clearly a major obstacle in implementing the Mitola's SDR for portable civilian use receivers.

4.2.2 Direct Conversion with Digital Front-End Decimation Architecture

As explained before, the ADC sample rate is locked to the maximum covered carrier frequency in Mitola's architecture. To break this lock, the Toshiba dualband

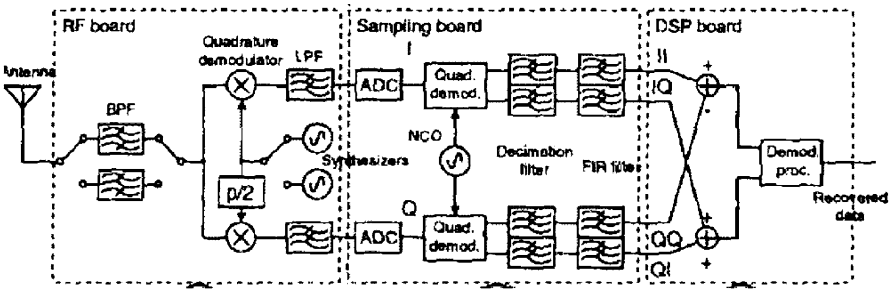


Fig. 4.3 Toshiba Direct-Conversion SDR-RX [14]: It covers both PCS and DCS bands. The entire band is first digitized and then a flexible digital front-end tunes to the individual channel of interest

SDR-RX [14] utilizes mixers to downconvert the carrier frequencies of the PCS (1.5 GHz) and DCS (1.9 GHz) bands to around DC (Fig. 4.3). This is in fact one step closer to conventional narrowband direct-conversion RX architectures [15], however what makes this architecture different from conventional thinking is that its inventors move most of the remaining usual analog blocks to the digital domain. The entire band of interest, consisting of at least 50 channels (about 10 MHz) is digitized in one piece. Then the digital front-end performs further downconversion, channel selection and the decimation tasks to tune to the desired channel. Analog front end consists of two RF band-select filters (for two bands: DCS and PCS), I-Q downconversion mixers, and 12-bit/64-MHz ADCs.

It should be noted that this is a low IF architecture with a variable IF frequency per channel. No image rejection filter is used and thus the typical required image rejection (e.g. 60−100dB) is not achievable. More importantly since one RF band select filer is needed per each band, this approach quickly becomes impractical if large number of bands is targeted, as is the case in SDR. At this stage the solution is either to design the programmable RF band select filters or to entirely remove the RF band select filter.

4.2.3 Sampler with Bulit-In Anti-Aliasing

In some early work on SDR-RX [16], Poberezhskiys opted to focus on removing the traditional RF preselect filter. They proposed to construct a programmable RF filter using the mixer (multiplier) as part of a sampler and weighted integrator (Fig. 4.4a). Although Poberezhskiys originally used different terms, we refer to this combination as weighted windowed integration sampler or in short windowed integration sampler (WIS).

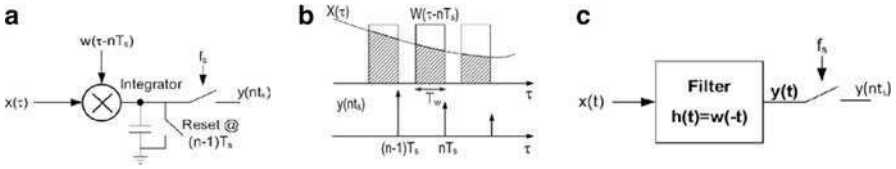


Fig. 4.4 (**a**) Windowed Integration Sampler (WIS) block diagram. (**b**) Graphical description of WIS operation principle. (**c**) WIS functional equivalent block diagram

4.2.3.1 WIS Operation Principle

A WIS integrates the multiplication result of a window waveform, $w(t)$ of length T_w, and the continuous-time (CT) input, $x(t)$, to generate one output sample (Fig. 4.4a). By shifting the window and repeating the multiplication-integration, output samples at any sampling moment (nT_s) can be calculated. This operation is formulated as follows:

$$y(t)|_{t=nT_S} = \int_{nT_s - T_w}^{nT_s} x(\tau)w(\tau - nT_s)d\tau \tag{4.2}$$

in which $w(t)$ is nonzero only over the time interval $[0, T_w]$. The graphical description of Equation (4.2) is shown in Fig. 4.4b. This equation can be rewritten as:

$$y(t)|_{t=nT_S} = \int_{-\infty}^{+\infty} x(\tau)w(\tau - nT_s)d\tau \tag{4.3}$$

Equation (4.3) shows that $y(t)$ is a convolution integral of $x(t)$ and $w(-t)$. Thus a more familiar interpretation of WIS can be represented by (Fig. 4.4c). Now it is clear that the continuous time input, $x(t)$, is filtered by a continuous time filter prior to being sampled. This is how WIS implements a sampler with built-in filter. The filter has a finite impulse response given by $w(-t)$ or equivalently a frequency response of $W(f)$.

4.2.3.2 RF-WIS Role in Wireless Receivers

If $W(f)$ has an RF bandpass filter shape, then WIS can act as an RF sampler – where the RF input is directly coupled to the WIS. Poberezhskiys [16] approximated $w(t)$ by a discrete waveform generated by a digital weight function generator (WFG). WFG can be programmed so that the RF bandpass filter tunes to the desired RF channel. Sampling rate can also be set to be lower than the RF signal Nyquist rate, and thus the sampled output is downconverted due to subsampling process [10]. With these choices, the traditional RF preselect filter, RF mixer, baseband filter and ADC sampler can be merged into a RF-WIS which is highly reconfigurable. This is

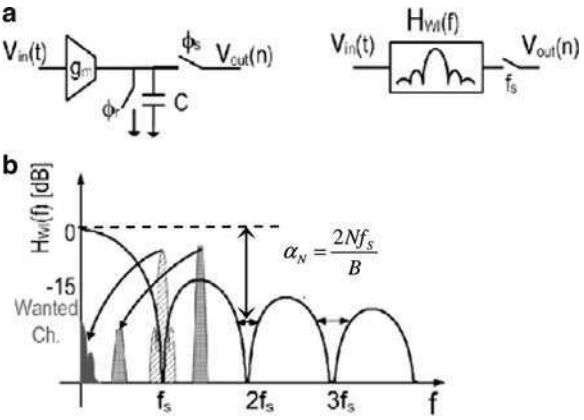


Fig. 4.5 (**a**) Rectangular WIS implementation, (**b**) Its first order $sinc(f)$ anti-aliasing response

a very powerful concept, but due to circuit imperfections satisfying the requirements of a wireless receiver with no RF preselect filter remains impractical [12].[1]

4.2.3.3 Baseband-WIS Role in Wireless Receivers

A baseband-WIS, where $W(f)$ has a low pass filter response, proves itself to be very effective for SDR-RX. Let's have a closer look to how baseband-WIS can be used in a wireless receiver. Yuan [18] implemented the simplest baseband-WIS, where $w(t)$ has a rectangular shape with $T_w = T_s$. The very simple implementation of rectangular WIS (RWIS) (Fig. 4.5a) and its interesting filter response are the key reasons to make it a practical and effective anti-aliasing sampler. As explained before the finite impulse response of the filter is given by $w(-t)$ and thus the RWIS built-in filter transfer function, in frequency domain, is given by (4.4) and plotted in Fig. 4.5b.

$$|H(f)| = \frac{g_m T_s}{C} \left| \frac{sin(\pi T_s f)}{\pi T_s f} \right| \tag{4.4}$$

As shown in Fig. 4.5b, the RWIS transfer function has a lowpass characteristic with a main lobe at DC and a set of side lobes rolling off at 20 dB/dec. It has zero response for those input frequencies residing at integer multiples of the sample rate, f_s. If the channel of interest properly lies at DC (or its vicinity) all the aliasing interferers will be around the nulls at Nf_s and strongly suppressed prior to sampling. Assuming a bandwidth of $\pm B/2$ for the desired channel and $f_s \gg B$, the minimum anti-aliasing stop-band attenuation of α_N around each null is given by (4.5):

$$\alpha_N = \frac{2Nf_s}{B} \tag{4.5}$$

[1] Accompanied by RF preselect filter, such RF samplers have been successfully implemented for fixed frequency narrowband receivers [17].

Equation (4.5) can be alternatively written as:

$$f_s = \alpha_N \frac{B}{2N} \tag{4.6}$$

From (4.5) it is clear that a higher sample rate provides higher attenuation for a given bandwidth. In other words one must choose a sample rate higher than the minimum required by Equation (4.6) for the specified antialiasing attenuation and bandwidth.

Other interferers, which are located in the side lobes but not on the nulls vicinity, are attenuated moderately and then fold down to the main lobe but away from the wanted channel at DC (Fig. 4.5b).

With the above description, it is clear that RWIS with its programmable built-in antialiasing filter fits very well into a wireless receiver to replace traditional impulse samplers. However, if all the anti-aliasing attenuation must be provided by the RWIS, it requires impractically high sample rates. For example, if 110 dB of suppression is needed over a 200-KHz bandwidth (as is the case in GSM), (4.6) dictates a sample rate of 30 GHz. Beside this impractical rate, circuit imperfections also limit the achievable null depths to around 50 dB [19]. Despite these limitations, RWIS is successfully used in UCLA SDR-RX as is explained shortly.

4.3 UCLA SDR-RX

Revised definition: Let us continue by highlighting that Mitola's SDR is by definition capable of receiving and transmitting multiple channels concurrently. In other word all the channels are digitized and available to the DSP at once, and the DSP can arbitrarily select any number of the channels per user request. This may be of interest to the military users but it is usually impractical and overkill (with resulting increase in complexity and power consumption) for portable civilian use cases. In civilian use of a personal communications device, the user knows beforehand what service he wants. Thus we find it more suitable to define the SDR as a radio platform which can be programmed to receive or transmit any *single channel*, with any modulation and located anywhere in a broad but finite predefined band. If two or more channels need to be received concurrently, then two or more of our type of SDR could be used in parallel with a possible sharing of some blocks. UCLA SDR-RX is designed based on this definition. The required SDR-RX flexibility must be offered at the low cost and low power consumption similar to those of the traditional *narrowband receivers*. The key points to low power narrowband design lies in the pre-ADC analog blocks acting as signal conditioner and delivering a well conditioned (low dynamic range) signal to the ADC (Fig. 4.6). On the other hand removal of the preconditioning blocks in favor of providing flexibility, in Mitola's SDR-RX, results in impractical ADC requirements with high power consumption. The main question will be how to make a balance and how

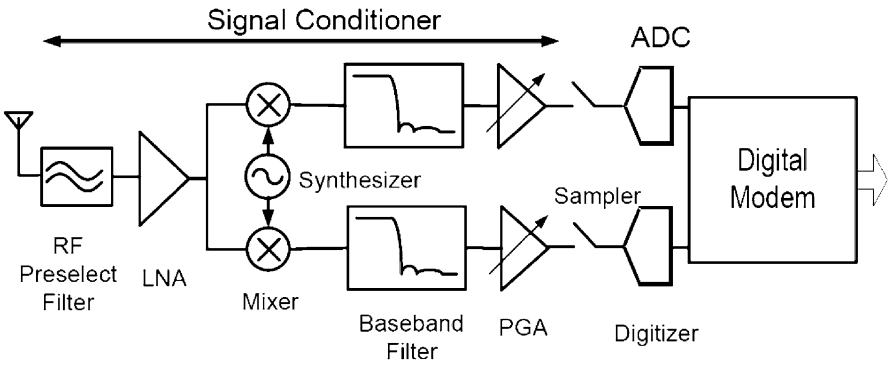


Fig. 4.6 Signal conditioning blocks in a narrowband receiver

much of the preconditioning must be preserved in analog domain. To answer the question, we first reexamine the essential tasks of the analog preconditioner in narrowband receivers.

4.3.1 Pre-ADC Analog Signal Conditioner in Narrowband Receivers

Figure 4.6 shows the main blocks of the pre-ADC signal conditioner. Downconversion, filtering and amplification are the three fundamental roles identified and briefly explained here.

Downconversion: For the ADC to operate at a low sample rate, the RF signal is downconverted to a lower frequency. Single-path downconversion by mixer transfers the signals from two different frequencies (one of which is wanted and the other of which is an image signal) to the same output frequency. Utilizing two-path downconversion (I and Q paths) is one way to deal with the image issue. Although IQ downconversion is theoretically image-free [20], in practice it provides a finite image rejection ratio (IRR) limited by the phase and gain imbalance of the I and Q paths. Direct conversion to zero IF[2] (ZIF-DCX) has the unique property that the image and wanted signal components belong to the same signal, and therefore its IRR requirement is much lower than the nonzero-IF case, where the image could be an unwanted signal of much higher strength.

Simple frequency planning and low IRR requirements have made the ZIF-DCX the dominant choice for modern receivers. For the rest of this chapter, we assume a ZIF-DCX architecture, although most of the ideas are applicable to low-IF direct conversion receivers too.

[2]Channel of interest after downconversion lies at DC.

Analog anti-aliasing filtering: Typically ADC has a delta sampler at its input and thus aliasing of the interferers located at multiples of the ADC sample rate can corrupt the wanted signal, unless the *anti-aliasing filter* suppresses those interferers. Thus anti-aliasing filters have been an essential part of the analog signal conditioners. Anti-aliasing filtering is accomplished by a combination of the RF preselect filter and the analog baseband filters, together implementing a brickwall LPF approximation.

Analog anti-blocking filtering: Strong interferers, not aliasing on top of the wanted channel at DC, must also be suppressed completely before demodulation. This is called *channel selection filtering*. Since demodulation is often performed after the ADC and in the digital domain, the channel selection could be achieved from RF preselect filter, analog baseband filters and digital filters. As it is explained later, trying to keep the analog section simple for our SDR-RX, we postpone much of the channel select filtering to digital domain. The question is how much, if any, of the filtering of non-aliased blockers must happen in analog domain? The answer becomes clear in noting that the ADC has a limited dynamic range. Nonblocking interferers must be attenuated to the extent that they do not overload the ADC, after they experience RX chain amplification gain. We identify this role as *anti-blocking filtering*, which is handled by the combination of all pre-ADC filters.

Amplification: The mixer and filters add noise to the tiny received signal, and thus the signal should be amplified significantly above the noise level of each block before it is fed to that block. This is how low-noise amplification becomes an essential task.

To adjust for the significant power variation of the received wireless signal, signal conditioning includes an automatic gain control (AGC) mechanism. AGC task is to set the gain of the analog front-end blocks so that the wanted-signal level at the ADC input remains well above the ADC in-channel quantization noise, and the total signal peak power (including blockers) at the ADC input is kept below the ADC full scale.

4.3.2 UCLA Low-Power SDR-RX: Architecture and System Design

Although ZIF-DCX narrowband architecture offers a simple and effective low-power single-mode radio, the following shortcomings make it ill suited for SDR-RX:

- Narrowband RX relies heavily on the RF preselect filter. Current technology doesn't allow for adjusting the center frequency or bandwidth of the preselect filter for different standards.
- Traditional LNAs are usually designed exploiting LC resonance phenomena and are only capable of amplifying the signal in a very narrow frequency spectrum.

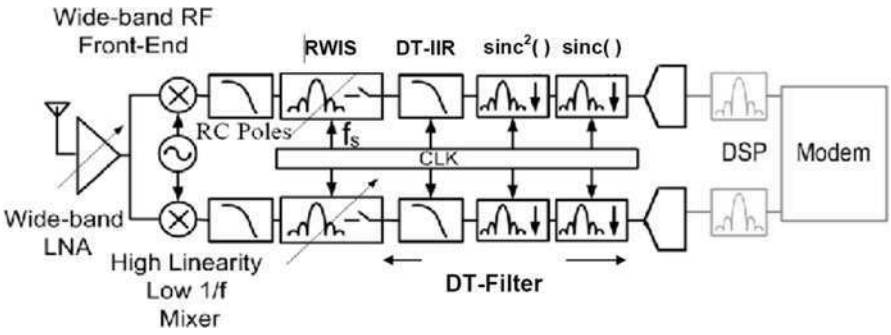


Fig. 4.7 RWIS-DTDec ZIF-DCX architecture for SDR-RX

- Conventional analog baseband filters require substantial design effort to meet the noise and linearity, and they are increasingly difficult to design in scaled technologies at low supply voltages. They are not easily tunable to address SDR-RX specifications.

To address the above limitations, we utilize the learning from previous SDR-RX examples and modify the narrowband architecture of Fig. 4.6 as follows. *First*, a shift from narrowband LNA and mixer design must be made to the truly wideband LNA and mixers. Wideband LNA design is the subject of Sect. 4.3.3.3. *Second*, the RF preselect filter is removed entirely. The absence of RF preselect filter and narrowband LNA rejection have significant influence on rest of the design. The immediate consequence is that a much stronger filtering is expected from the baseband filters. Furthermore very high linearity requirement is imposed on the RF/analog blocks, particularly on the downconversion mixer. In addition, harmonic mixing in the mixer should be eliminated or highly reduced. *Third*, an ADC which has a dynamic range higher than the minimum requirement (of the narrowband receiver ADC) is selected. The extra dynamic range is utilized to relax the analog filter and VGA requirements by pushing these tasks partially into the DSP domain. It should be noted that although the increase in ADC dynamic range helps with anti-blocking and channel selection requirements of the analog filters; it does not help to lower the antialiasing requirements. The aliasing of interferers happens in the course of sampling and there is no way to undo the aliasing distortion in the digital domain. *Fourth*, conventional analog baseband filter and the delta sampler are replaced with windowed integration sampler- which, as explained before, offers strong antialiasing filter with high degree of re-configurability. *Fifth*, to ease the WIS requirement a passive RC filter (say 2nd order) is introduced as part of the mixer load. This relaxes both the linearity and filtering requirements of the WIS, in particular the antialiasing requirement.

The proposed SDR-RX block diagram is shown in Fig. 4.7. Design choices are further explained and quantified in following sections.

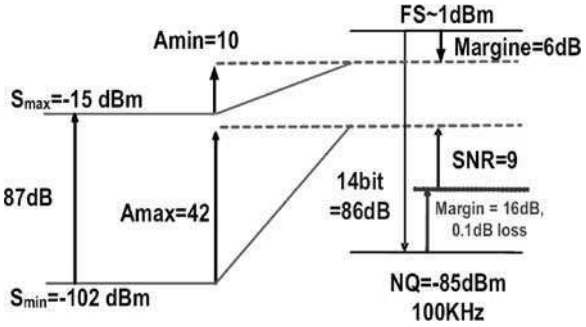


Fig. 4.8 Programmable gain amplification requirement for GSM example

4.3.2.1 Low Power ADCs at Baseband

As explained before a high dynamic range ADC is desired, as long as its power consumption is acceptable. Let us budget 10 mW of power from a 1-V supply to the ADC. Going by recent publications, at this power consumption it is possible to realize a 9-bit, 40-MHz Nyquist ADC, or a 14-bit, 100-kHz noise-shaped delta-sigma ADC that samples at 9 MHz. We assume that both ADCs are available and that one or the other is chosen based on the wanted channel bandwidth and blocker profile. It is also reasonable to assume that low power reconfigurable ADCs could be used to offer programmable number of bits (in trade off with channel bandwidth) in between these two ADCs.

4.3.2.2 Absorbing Variable Gain into ADC

As the first example of lowering the analog complexity by utilizing the DSP or "digital as much as possible", let us determine the minimum analog VGA requirements. We will look into GSM and 802.11 g requirement.

According to the GSM standard, the channel of interest can be anywhere from −102 to −15 dBm in strength at the receiver antenna (Fig. 4.8). This is an 87-dB dynamic range. Starting from the A/D converter, we assume the 14-bit resolution ADC is selected and it has +1 dBm (0.5 V, peak-to-peak) full scale power. The quantization noise floor in the 100-kHz bandwidth of the GSM channel is then at −85 dBm. GSM needs a detection signal-to-noise ratio (SNR) of 9 dB, so if quantization noise sets the noise floor at the ADC input, the RF/analog sections prior to the A/D should amplify by 26 dB. However, in reality, thermal noise in the receiver front-end sets the detection SNR, and to limit further degradation by quantization noise to only 0.1 dB, the signal must be amplified by another 16 dB, leading to a maximum gain of 42 dB (Fig. 4.8).

If the receiver gain were to remain constant at 42 dB, the largest GSM input signal would overload the ADC. For large inputs, gain must be lowered from 42 dB to 10 dB, which leaves a 6-dB margin below the ADC full scale, allowing for the envelope variations in EDGE and PGA gain setting error. Thus, by exploiting

the available A/D dynamic range, a 32-dB variable or programmable gain in the receiver's RF/analog portion is sufficient to capture a single input channel with an 87-dB dynamic range; the DSP absorbs the remaining 55 dB.

Similarly, the minimum range for RF/analog variable gain can be found for 802.11 g reception. For this wideband system, the minimum detectable signal at the receiver input is −82 dBm in normal mode, and −65 dBm at high data rate. The largest input signal is −20 dBm. The 9-bit and 40 MHz ADC is used in this mode. Allowing for the 26-dB required SNR for detection at an acceptable error rate, and given the smaller dynamic range of the ADC than for GSM, the RF/analog gain should be variable from 8 dB to 47 dB. In the wideband case, then, the analog part carries a larger burden. This is a reasonable trade-off; because to shift the burden to DSP would cost a disproportionate rise in A/D power consumption.

4.3.2.3 Programmable Baseband Filter with RWIS Core

A combination of the passive RC filters, rectangular windowed integration sampler (RWIS), discrete-time analog IIR (DT-IIR) and the discrete-time analog decimation filters (DTDec) provides very strong programmable filter solution. We refer to the combination of the last three as RWIS-DTDec. RWIS-DTDec filter architecture block diagram is shown in Fig. 4.7. The RWIS is clocked at an initial sampling frequency f_s and as explained before it introduces a continuous-time (CT) filter with $sinc(f)$ response with nulls at f_s and its integer multiples. Combination of the RC filter and RWIS offers the required antialiasing rejection. Usually the initial sampling-rate, f_s, is in the range of few-100s MHz and relatively large compared to the desired signal bandwidth, because for a given signal bandwidth the higher sampling frequency results in a higher attenuation around the null (4.5) and from the RC filter. Therefore analog decimating filters are needed to lower the sampling rate to a range suitable for low power ADC.

In addition, strong non-aliased blockers in the sidelobes dictate a very high dynamic range for the following ADC. The DT-IIR lowpass filter (Fig. 4.7) attenuates these blockers and helps in the anti-aliasing suppression needed by the following decimators. This filter is easily implemented as part of RWIS circuitry as shown later. Then, the signal passes through a second-order anti-aliasing DT-FIR filter with $sinc^2(f)$ response followed by a decimation of four. In the last stage, the signal is filtered and decimated one more time – with a selectable decimation of three for 802.11 g or two for GSM. The selection criteria for the synthesized structure will be made clearer in the next section.

As will be described in Sect. 4.3.3, the RWIS-DTDec combination is mainly composed of switches and capacitors, so it has high linearity and a high degree of scalability with technology. RWIS-DTDec filter response is only a function of clock frequency and capacitor ratios. So it is highly programmable and insensitive to process-voltage-temperature (PVT) variation. Furthermore the WIS also serves

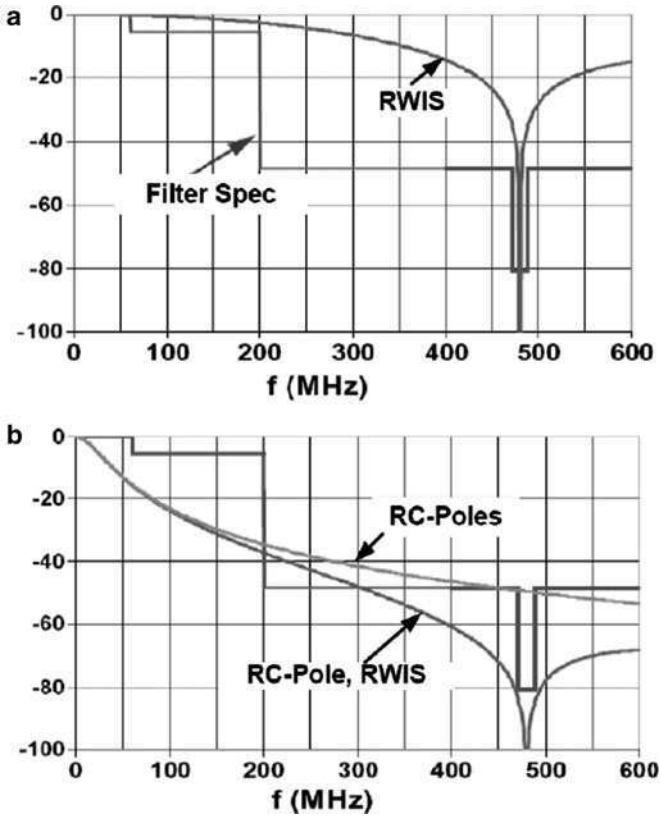


Fig. 4.9 RWIS-DTDec filter design illustration-I; RWIS and RC poles are included

as an amplifier whose gain is set by the capacitors and clock frequency. The clock frequency is chosen to meet the filter requirements, but the capacitor value is then set to control the gain as part of the PGA.

4.3.2.4 Examples of Synthesis of RWIS-DTDec

In this section we show, in detail, the evolution of the sampler and filter for the 20-MHz wide 802.11 g channel as a series of plots (Figs. 4.9, 4.10 and 4.11). On each plot, the filter requirement template, the individual filtering response of the added stage, and the overall cascaded response are plotted.

802.11 g channels span from 2.4 to 2.48 GHz. The nearest well-specified out-of-band blockers are strong cellular channels in the 1.9 GHz CDMA band. To protect the minimum high data rate 802.11 g channel of −62 dBm from suffering co-channel interference due to aliasing, all CDMA channels (with −15 dBm power)

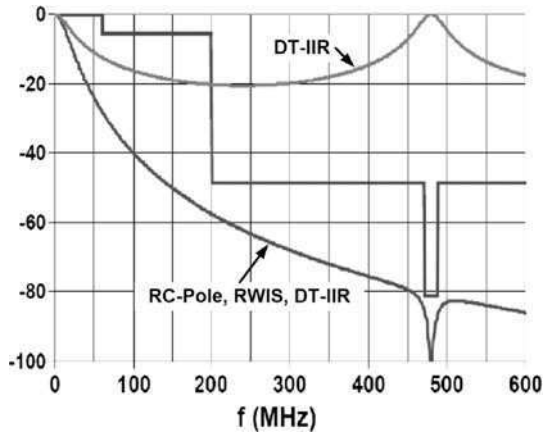


Fig. 4.10 RWIS-DTDec filter design illustration-II; DT-pole effect is added

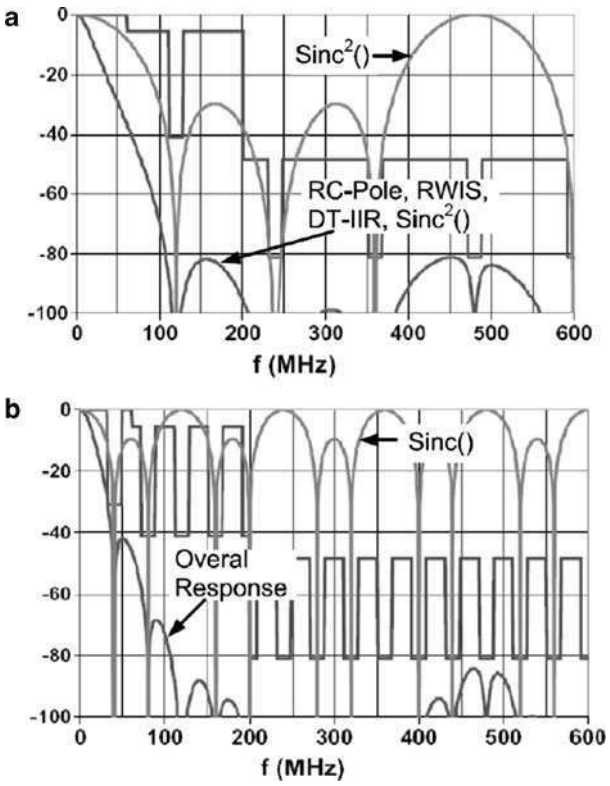


Fig. 4.11 RWIS-DTDec filter design illustration-III; decimation filters are added

in a contiguous 16-MHz-wide band at an offset equal to the sampling frequency or its multiples must be suppressed by 80 to 83 dB. This results in a filter specification with deep nulls at all aliasing frequencies (Fig. 4.9a). Search by trial and error leads

to an initial sample rate of 480 MHz. This high rate widens the sampler's stopband, although not enough for 80-dB attenuation across 16 MHz that requires a much higher rate (Fig. 4.9a).

The two-pole passive RC filter with a cutoff frequency beyond the channel of interest at zero IF, say at 20 and 40 MHz, attenuates blockers around the null at 480 MHz by another 50 dB to meet the specification (Fig. 4.9b). RC poles are chosen high enough so that, even with high PVT variations, in-channel droop remains negligible. However, the filter violates the specification at offsets of 200–300 MHz. This region lies at roughly half the sample rate, and coincides with the Nyquist frequency at the sampler output. Now we turn to utilize the DT-IIR filter stage. The DT pole magnitude response is uniquely defined up to input frequencies equal to the Nyquist rate, followed by images around the clock frequency and its multiples (Fig. 4.10). Thus, it has minima in its magnitude characteristic at the Nyquist rate and odd multiples. With an adjusted pole frequency of 13 MHz, the filter minimum at 250 MHz is at −20 dB. This pole is placed precisely, independent of PVT variations. In cascade with the sampler frequency response, this meets the filter specification everywhere (Fig. 4.10).

But, our task is not yet complete; for 480 MHz is too high a rate for digitization by a low-power ADC. The rate must be lowered by the decimating filter. With each downsampling by M, the number of anti-aliasing notches in the specification also multiplies by M. A decimation filter of the right order to fulfill the specification is again found by trial-and-error. In general, the larger the downsampling factor M, the higher the order of the required filter. It is cumbersome in practice to realize a filter of order higher than 2. For 802.11 g, then, with a $sinc^2$ decimation filter the downsampling is limited to 4x (Fig. 4.11a). Now the sample rate is 120 MHz, but this is still too high. The filter's output must be downsampled again, and this time it can be downsampled by 3x using a first-order sinc decimation filter (Fig. 4.11b). The final sample rate is 40 MHz, which can be easily digitized at 9-bits resolution by a Nyquist ADC.

Using the same design process, GSM can be received in the presence of 0-dBm blockers (as high as −53 dBm/Hz blocker power spectral density) with the same hardware described above, but with different clock rates and a slight reconfiguration, as follows. An initial sampling by windowed integration at 72 MHz is followed by downsampling by 4x with $sinc^2$ filtering, and downsampling by 2x with $sinc$ filtering. The output sample rate is 9 MHz, which is very reasonable for a milliwatt delta-sigma ADC that resolves 14-bits in a 100-kHz bandwidth. The two-pole passive RC filters cutoff frequencies are switched to about 550 KHz and 1.1 MHz.

4.3.3 UCLA SDR-RX: Circuit Realization

In this section we look into the design of the circuit blocks enabling UCLA SDR-RX. First we present the RWIS-DTDec filter circuit and then wideband RF front-end circuit is described.

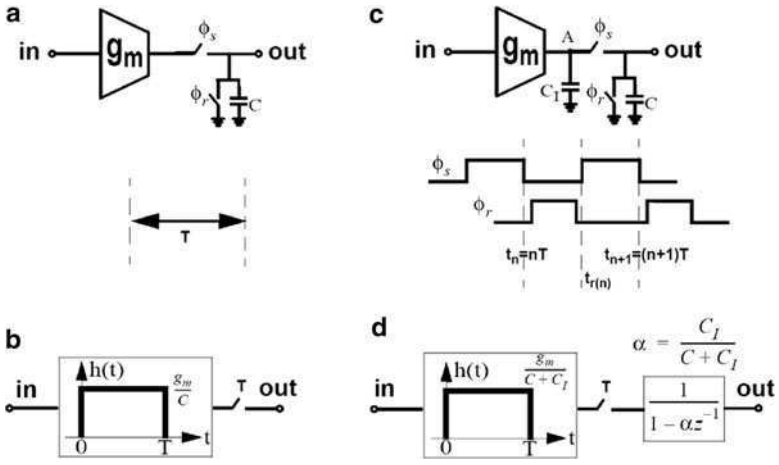


Fig. 4.12 Filter circuit and block diagram: (**a**, **b**) Simple RWIS. (**c**, **d**) RWIS and DT-IIR combo [48]

4.3.3.1 RWIS-DTDec Filter Circuit Realization

The cascade of RWIS and DT-IIR filters in Fig. 4.7 can be implemented easily and compactly using a single transconductor and a combination of capacitors and switches (Fig. 4.12). We note that the continuously connected parasitic capacitance at the output of the transconductor (C_I in Fig. 4.12c), in parallel with the resistance of the periodically switched sampling capacitor (C in Fig. 4.12c), forms a discrete-time pole. In other words since C_I is not reset to zero at each clock it carries on its charge which is proportional to the previous output sample for the next integration period. This will lead to:

$$V_o(n+1) = \frac{C_I}{C+C_I} V_o(n) + \frac{g_m}{C+C_I} \int_{nT_s}^{(n+1)T_s} V_{in}(t)\,\mathrm{d}t \tag{4.7}$$

which is mapped to the equivalent system in Fig. 4.12d.

From (4.7) the DT-IIR filter pole in the z-domain is located at $\alpha = C_I/(C + C_I)$, which is mapped to a 3-dB cutoff frequency of $(C/2\pi C_I)f_s$ in Hertz. As this is a discrete-time pole, its magnitude response is uniquely defined up to input frequencies equal to the Nyquist rate, followed by images around the clock frequency and its multiples. Thus, it has minima in its magnitude characteristic at the Nyquist rate and odd multiples. For 802.11 g reception, we set the DT-IIR 3-dB cutoff frequency to 12.2 MHz ($\alpha \approx 0.86$), and that of GSM is set to 460 KHz ($\alpha \approx 0.96$). To achieve these values, another capacitor is added to the output parasitic capacitance of the transconductor. Since this cutoff frequency is controlled with the clock and capacitor ratios, it is precisely controlled and does not change with PVT variations.

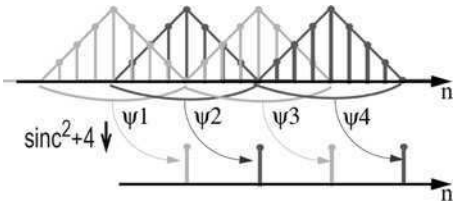


Fig. 4.13 Time domain interpretation of $sinc^2$ filter response followed by a decimation by four

To implement the DT-FIR $sinc^2$ filter with nulls at $f_S/4$, let's write its z-domain transfer function:

$$H_1(z) = \left(\frac{1-z^{-4}}{1-z^{-1}}\right)^2 = 1 + 2z^{-1} + 3z^{-2} + 4z^{-3} + 3z^{-4} + 2z^{-5} + z^{-6} \tag{4.8}$$

The time-domain interpretation of this transfer function, including the decimation by four, is demonstrated in Fig. 4.13. Each output sample is derived through a triangular weighted summation of the current and six previous input samples, evident from (4.8). Because decimation by four is included, the triangular window is shifted over four input samples and the next output sample is constructed by a new weighted summation (Fig. 4.13).

Moreover, as graphically shown, each input sample is used in the generation of two output samples, and its total weight for all input samples is four. This means that capacitor banks consisting of four equal capacitors can be used to store output samples of RWIS and DT-IIR and then part of the bank can be used in generating one $sinc^2$ output sample with the remaining capacitors to be used in the generation of the next sample. This approach has been utilized to implement the compact architecture of Fig. 4.14 for the second-order FIR filter and its built-in decimation by four.

As illustrated in Fig. 4.14, there are eight parallel paths of capacitor banks with four identical capacitors in each. At each clock cycle, one path is rotationally selected and its four parallel capacitors are reset and connected to the transconductor output (Fig. 4.15). At the end of the clock cycle, these four capacitors have identical stored charges which result from the integration of transconductor output current and charge-sharing with C_I. Thus, the charge of each capacitor corresponds to the output sample of cascaded RWIS and DT-IIR.

In the meantime, at appropriate phases, proper numbers of capacitors from each capacitor bank of the seven remaining paths (shown in Fig. 4.14) are connected to a pre-discharged capacitor of the next stage to create the desired sample after triangular weighted charge-sharing similar to Fig. 4.13. The unused number of capacitors from each capacitor bank will be used in next clock cycle. In this way, the decimating-by-four DT-FIR $sinc^2$ filter is compactly realized.

The next and final filtering stage is the first-order DT-FIR sinc filter followed by a proper decimation, but decimation should be selectable between three or two as explained before. If the decimation factor is three, the proper filter transfer function is:

$$H_2(z) = \frac{1-z^{-3}}{1-z^{-1}} = 1 + z^{-1} + z^{-2} \tag{4.9}$$

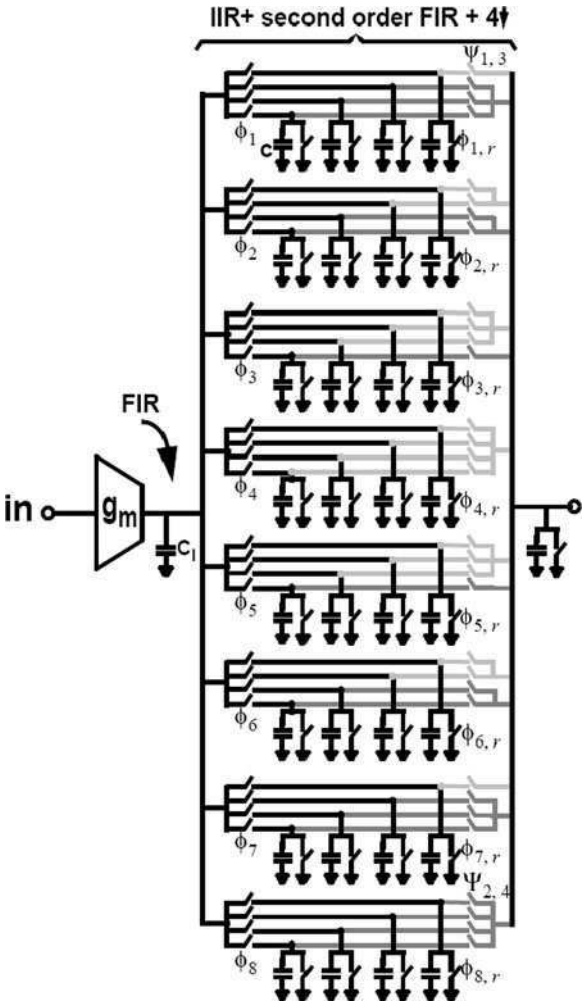
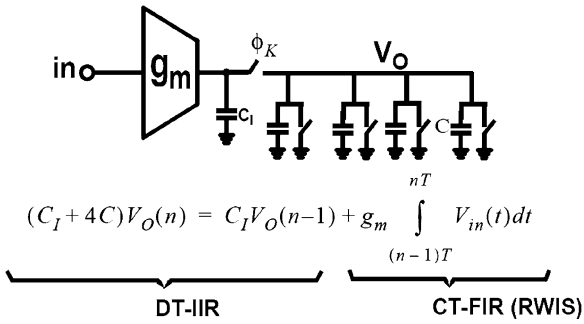


Fig. 4.14 The circuit of RWIS, DT-IIR and decimating by four *sinc*^{2} filter; single-ended presentation



$$(C_I + 4C)V_O(n) = C_I V_O(n-1) + g_m \int_{(n-1)T}^{nT} V_{in}(t)dt$$

Fig. 4.15 Creation of CT-FIR and DT-IIR stored in the capacitors of each path in Fig. 4.14

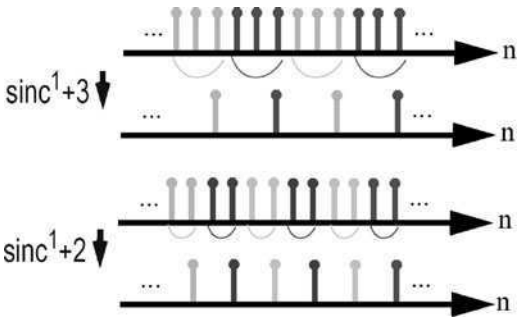


Fig. 4.16 Time domain representation of sinc filter and following decimations

The required transfer function for decimating by two is:

$$H_2(z) = \frac{1 - z^{-2}}{1 - z^{-1}} = 1 + z^{-1} \tag{4.10}$$

The time-domain representations are depicted in Fig. 4.16. The first-order *sinc* filter turns into a uniformly weighted summation of consecutive samples, which can easily be done by shorting the capacitors holding these values. After charge-sharing, the final value is the desired sample. This leads to the final implementation shown in Fig. 4.17, in which all of the capacitors in the $sinc^2$ and $sinc^1$ filters have the same sizes. The actual implementation is differential with differential capacitors to save silicon area and to make it robust to common-mode noise sources, clock feedthrough, and charge injection. It should be highlighted that nonlinearity stemming from charge-injection is not important in this filter, and the filters nonlinearity is merely dictated by the transconductor [19]. Consequently, there is no need for clock boosting, and a simple clocking scheme is good enough. The required clock phases are shown in Fig. 4.18 [21].

4.3.3.2 Gain Programmability of RWIS-DTDec Filter

Using (4.4) for RWIS gain and including the attenuation resulting from the following charge sharing actions, the total DC gain of the filter in Fig. 4.17, from the continuous-time input to the discrete-time output, is:

$$G_{DC} = \frac{g_m T_s}{4C} \frac{16}{17} \tag{4.11}$$

As a result, taking advantage of switchable transconductors and capacitors makes this architecture very well suited for gain programmability. The transconductor is composed of parallel combination of four identical transconductors, that can be independently powered up/down. Similarly, each of the capacitors is composed of parallel combination of eight identical smaller capacitors. By turning four identical transconductors on and off and by switching in and out of eight unit capacitors,

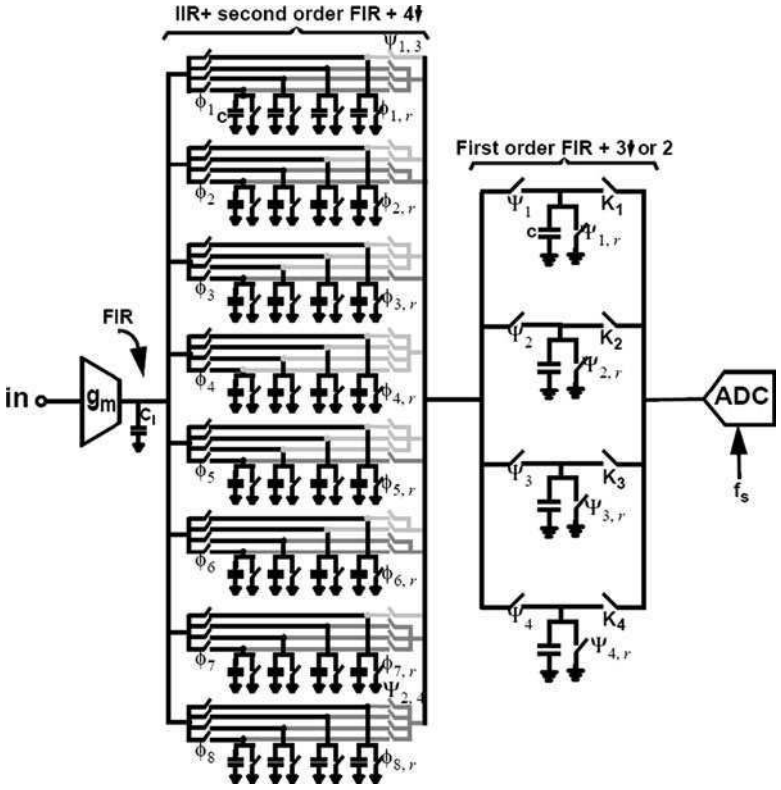


Fig. 4.17 RWIS-DTDec filter complete circuit; single ended presentation

30-dB gain variations with 6-dB steps are manifested. The size of a unit capacitor for 802.11 g case is 200 fF and that for GSM is 400 fF. This means that, for GSM, the size of capacitor C is selectable from 400 fF to 3.2 pF, whereas for the 802.11 g, this capacitor varies from 200 fF to 1.6 pF. Since gain-adjusting should not dislocate the DT-IIR pole location, the capacitor, C_I, is also switched accordingly. This dictates a total capacitor of around 435 pF for the filter, which occupies an area of about $500 \times 500\,um^2$ using MIM capacitors with 2-fF/um^2 density. For GSM, with an initial sampling rate of 72 MHz, the gain varies from 6 dB to 36 dB, compared with gain variations of -4 dB to 26 dB in 802.11 g, with 480 MHz of initial sampling.

4.3.3.3 Wideband Radio Front-End Circuits

This SDR receiver needs a wideband low noise amplifier (LNA) which gives a relatively uniform gain and input impedance close to 50 Ω over 800 MHz to 6 GHz spectrum. The LNA and mixer must handle the full dynamic range of the wideband spectrum incident to the antenna, without circuit distortion corrupting the wanted

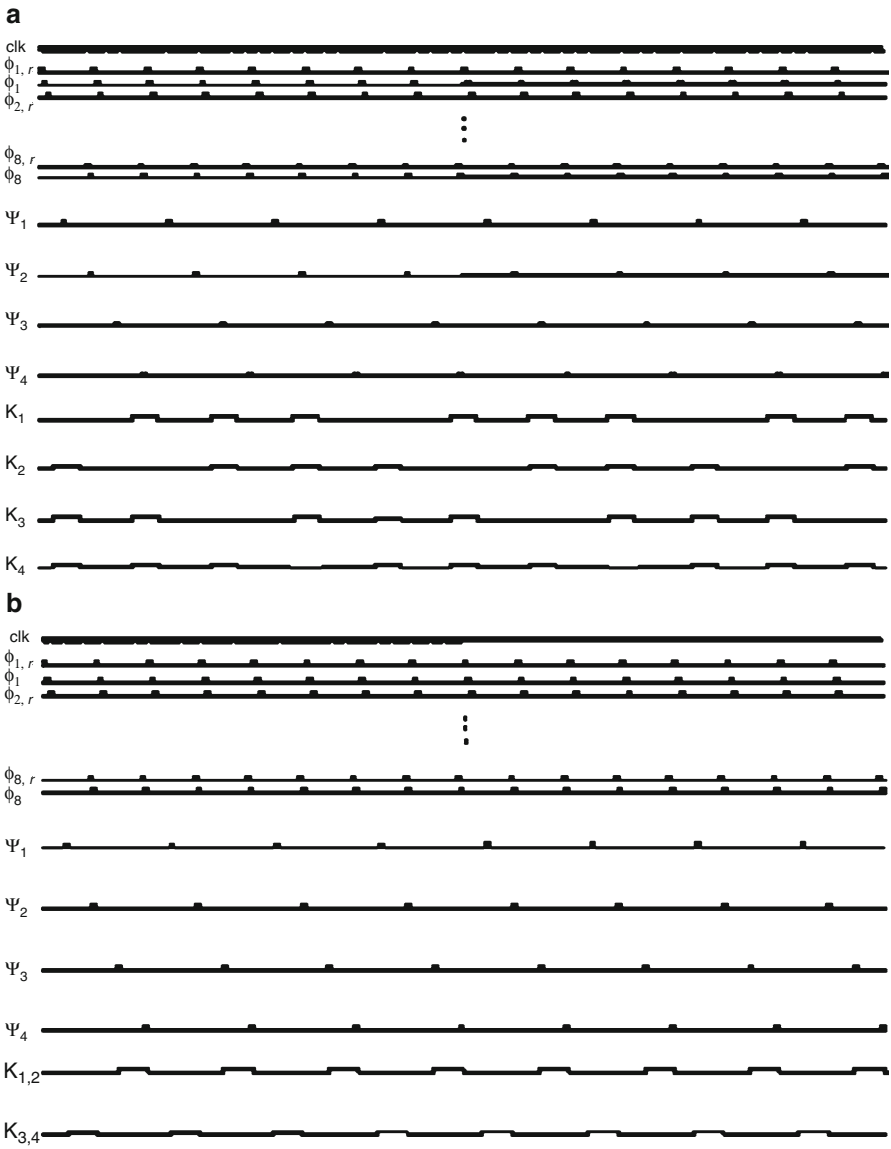


Fig. 4.18 Required clock phases: (**a**) 4–3 decimatio n mode, (**b**) 4–2 decimation mode

signal. The LNA must be wideband at input and output ports, and the mixer should be wideband at its input and LO ports. The output of the mixer is narrowband lowpass, because the wanted channel is at zero IF. A wide-tuning-range synthesizer must provide an LO signal which varies from 800 MHz to 6 GHz.

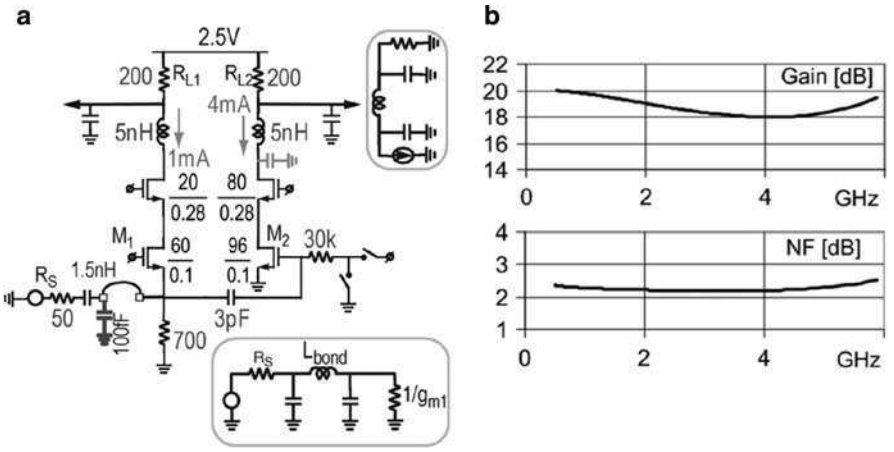


Fig. 4.19 Wideband LNA. (**a**) Circuit and LC ladder bandwidth extension. (**b**) Gain and noise figure

Noise-Cancelling Wideband LNA

The narrowband LNA design benefits significantly from resonant circuits at its input and its load to achieve a high gain, low noise figure and impedance matching. But a wideband LNA must provide high gain, a low noise figure and also acceptable 50 Ω input impedance matching over many octaves. This requires design techniques and circuit configurations different from traditional narrowband examples. Conventional wideband amplifiers are either distributed or use resistive feedback to attain the broadband features. The distributed approach often suffers from high power consumption and low gain [22, 23].

It is well recognized that the common gate (CG) LNA presents a broadband resistive input impedance and a noise factor of $1 + \gamma$, which is usually larger than 3 dB for short channel MOSFET devices. In wideband use, it also suffers from a low voltage gain. For a given capacitive load, say due to the following mixer, the load resistance must be lowered to push out the output pole. With a typical capacitive load of 100 to 150 fF, an LNA resistive load of 200 to 250 Ω can be chosen. Considering a 200 to 250 Ω resistor as load and matching the LNA input to 50 to 60 Ω, the LNA insertion gain will be around 12 dB. As a result of this low gain, the load resistor noise contribution is more visible and raises the total noise figure to about 5 dB. This makes CG-LNA ill-suited for high-sensitivity wideband applications.

To increase the wideband gain, the proposed LNA includes a single-ended to differential conversion, consisting of common gate (M_1) and common source (M_2) stages in parallel (Fig. 4.19). Compared to the CG-LNA, this can raise the LNA gain by up to 6 dB when the output swings are balanced. Load resistor noise is also less significant due to higher available gain. However, this circuits most important property is that noise from M_1 can be nulled [24, 25].

The insertion voltage gain of this LNA under general conditions is:

$$A_v = g_{mt1}R_{L1} + g_{m2}R_{L2} \tag{4.12}$$

The first term is due to gain in the CG stage, and the second term is the CS gain. g_{mt1} is the total transconductance of M_1, including the body effect, and is set to 20 mS to match $R_s = 50\,\Omega$. The resistance of the two loads, R_{L1} and R_{L2} (Fig. 4.19), is limited for a given next-stage capacitance by the desired upper cut-off frequency (f_u).

The interesting property of this circuit is that the fraction of M_1 noise current that flows into R_{L1} and R_s induces, by driving the gate of M_2, an in-phase amplified noise current in R_{L2}. Neglecting delays in the signal path, if the resulting noise voltages at the two output terminals are equal, then the noise of M_1 is common-mode and is nulled by differential sensing [25].

With a desired upper cutoff frequency of 6 GHz, FET and parasitic capacitances, as well as parasitic inductances due to bondwires, can be a major limitation. Instead of trying to minimize these parasitics which soon reaches a point of diminishing returns for the effort involved, it is more productive to embed them into a well-understood network with desirable properties. In this case, as the signal enters the amplifier, it sees, first, the lead parasitic capacitance to ground, then a series bondwire inductance, then the pad capacitance to ground in parallel with C_{GS} of the C-G and C-S FETs. Terminating this is the resistance $1/g_{mt1}$. In this configuration, the elements resemble a doubly-terminated all-pole third-order LC ladder filter. By adjusting the component values in simulation, one can approximate a maximally-flat transfer function. This embedding can improve the bandwidth of acceptable impedance match, that is when $S_{11} < -10\,\text{dB}$ by as much as two octaves. It also removes droop in the transfer function from v_s to v_{gs1} and v_{gs2}. The desired effect is obtained in this amplifier by adjusting the FET sizes, thus their C_{GS}, and effective gate bias voltages. The same concept can be applied at the load resistor, which drives the input capacitance of the mixer. A broadbanding effect is obtained by inserting 5-nH on-chip spiral inductors strategically at the drains of the cascode FETs to form a singly-terminated third-order maximally flat LC ladder low-pass filter. Again, this extends the useful bandwidth significantly.

Mixer

The passive mixer core, driven by a sharp-edged LO, presents a very low 1/f noise. But it is hard to realize a voltage excitation at RF to drive the mixer core. In other words, the LNA output is usually high impedance and cannot be approximated by a voltage source. So we decided to drive the passive mixer by a current source. This is, in principle, possible because of true-switch nature of the four-FET mixer. A transconductor is used to convert LNA output voltage to a current and feed it to the mixer. The mixer output port delivers the commutated current to the next stage. It is possible to convert this current into voltage by connecting a simple impedance to

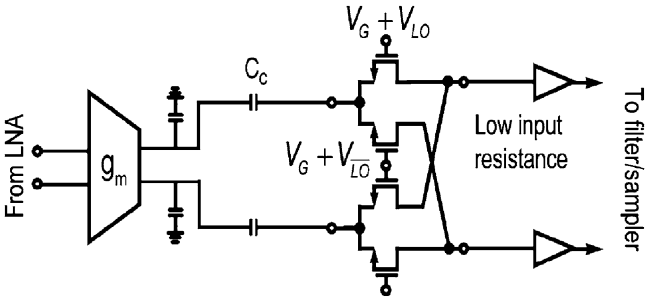


Fig. 4.20 High linearity and low 1/f-noise current driven passive mixer circuit

mixer output. But the high input impedance of this stage usually upsets the current source, and in our case it degrades mixer linearity and noise performance. This high impedance causes voltage swing on mixer (core) input/output ports, and this voltage swing generates flicker-noise-dependent current flow to finite impedance seen at the mixer (core) input node. This is similar to the indirect mechanism described in [26] for active mixers which are current driven too.

This problem is solved by using a transimpedance stage, which by definition has low input impedance, as mixer load [27, 28]. The completed circuit embeds the mixer core between a transconductor at the input and a transimpedance buffer at the output (Fig. 4.20). The transimpedance feedback amplifier or, more straightforwardly, a common-gate FET amplifier with a small input impedance, can be used for mixer output.

It is assumed that in the pure current commutating mixer, only signal-bearing RF current, but no bias current, flows through the switches. This means that the input transconductor should provide an internal path for bias current to flow from supply to ground without passing through mixer switches. With the above considerations, Mixer FET-switches commutation happens mostly in triode region and thus the FET-switch flicker noise and *Vth* mismatch have zero transfer gain to the mixer output. This simply results in low flicker noise and high linearity.

Another problem associated with a wideband receiver is that when the LO tunes a channel at the lower end of the receiver passband, the square wave commutation mixes unwanted channels at the LOs third and fifth harmonics, which also lie in the passband. These channels also appear at zero IF. This effect can only be suppressed by somehow "linearizing" the LO port, but a hard-switching mixer is always preferred because it gives the best conversion gain and noise performance. The harmonic content associated with the hard switching can be lowered by shaping the commutation square wave into a stepwise waveform resembling a sinewave; more precisely, a waveform that corresponds to samples of a sinewave. This is obtained by constructing a mixer from weighted transconductors in the ratios of $1{:}\sqrt{2}{:}1$, whose output currents are switched by LO waveforms delayed by one-eighth of the period and added together (Fig. 4.21). Theoretically this commutation

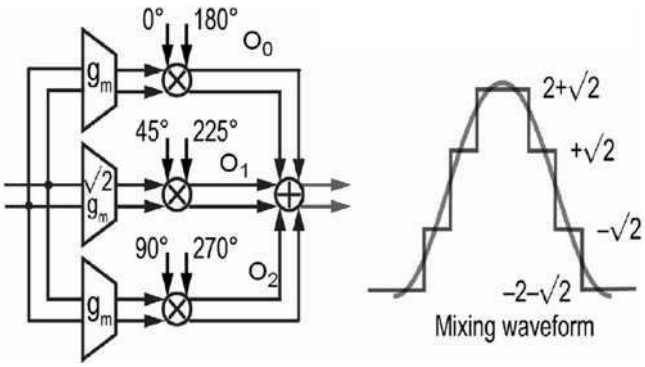


Fig. 4.21 Harmonic suppressing mixer block diagram and its sinusoidal approximated mixing waveform

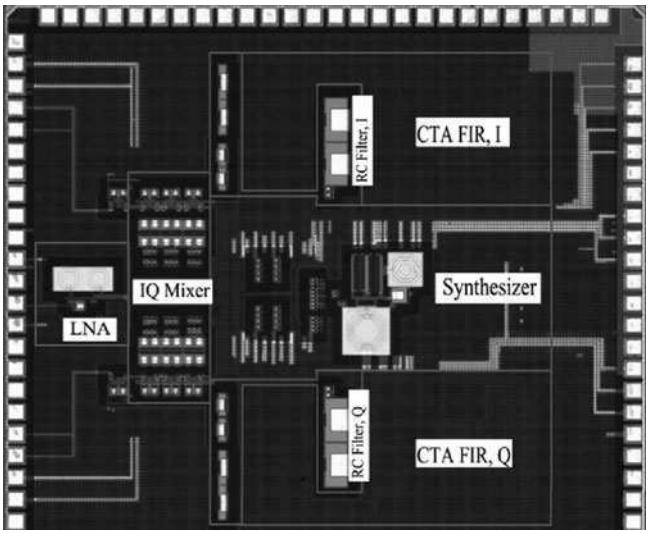


Fig. 4.22 Die photo

waveform has no third or fifth harmonic [29]. But in practice, phase and amplitude error of the three phases will result in a limited achievable harmonic rejection [25]. Harmonic rejection mixer block diagram is shown in Fig. 4.21.

4.3.4 SDR-RX Prototype

The prototype SDR-RX was fabricated in ST Microelectronics 90-nm CMOS process. Active area is 3.8 mm^2, which is mostly occupied by the baseband filter capacitors (Fig. 4.22).

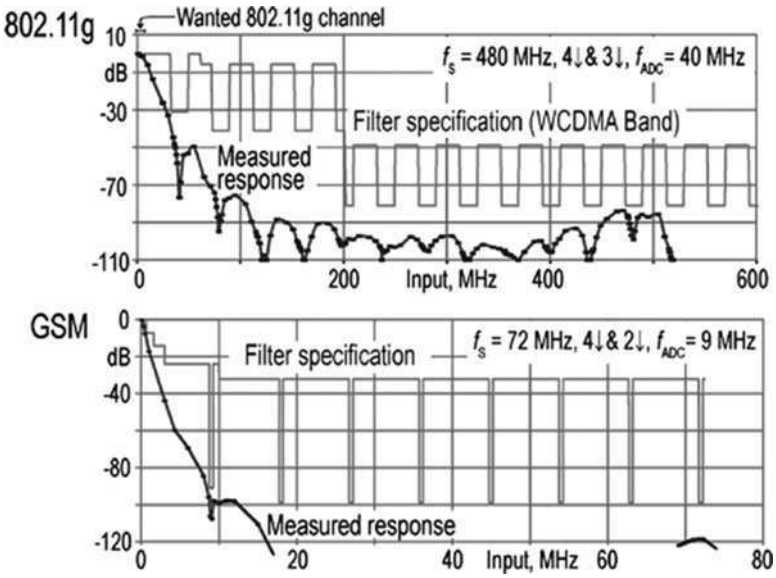


Fig. 4.23 Measured selectivity of the receiver for GSM and 802.11 g modes

Measured overal filter response for 802.11 g and GSM is plotted against the specifications, showing the deep anti-aliasing notches (Fig. 4.23). The passive mixer load was switched between poles at 20 and 40 MHz for 802.11 g and 550 and 1,100 kHz for GSM reception. The specifications are met with margin, clearly demonstrating that the required selectivity can be achieved without the RF prefilter and narrowband LNA rejections. RF front-end measurement results are given in [12, 25].

4.4 Summary

In this chapter an overview of previously introduced SDR-RX architectures was presented. A novel architecture for low power SDR-RX architecture was described and it was explained how this architecture is evolved based on the learning from prior SDR-RX design efforts and the narrowband receiver architectures. It was highlighted that ADC-centric design is the key point to low power wireless receiver design, meaning that the proper pre-ADC analog signal conditioner must be incorporated into the design. Windowed integration sampler, with its built in anti-aliasing filter and as a replacement for traditional delta-sampler, offers the high degree of programmability required in a low power SDR-RX signal conditioner. Examples of circuit realization for the programmable filter and wideband front-end in a fully integrated CMOS SDR-receiver were described, demonstrating that the required selectivity can be achieved with no RF preselect filter. However

improvement in the performance of this SDR-RX in the presence of strong blocking interferers (in the absence of RF preselect filter) is required [12]. This requires better linearity performance from RF-FE and particularly from the wideband mixers. Current driven passive mixer [25, 28] seems to have high potential in this regards and is the subject of extensive research these days.

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Chapter 5
Interference Rejection in Receivers by Frequency Translated Low-Pass Filtering and Digitally Enhanced Harmonic-Rejection Mixing[1]

Eric Klumperink, Zhiyu Ru, Niels Moseley, and Bram Nauta

5.1 Introduction

Software-Defined Radio (SDR) and Cognitive Radio (CR) concepts have recently drawn considerable interest. These radio concepts built on digital signal processing to realize flexibly programmable radio transceivers, which can adapt in a smart way to their environment. As CMOS is the mainstream IC technology for digital, we would also like to realize SDR and CR radio transceivers in CMOS. Attempts are being made to integrate the functionality of multiple dedicated narrowband radios into one radio chip, which is reconfigurable by software [1, 2]. This is hoped to bring cost and size reductions while supporting an ever increasing set of communication standards in a single device. The SDR concept might also allow field upgradable radios to accommodate evolving standards or cognitive radios to improve the efficiency of spectrum use [3].

To support the reception of a wide range of radio signals at different frequencies, a wideband radio receiver seems an obvious solution [4, 5]. Not only for SDR applications such receivers have been proposed, but also for instance for TV reception [6, 7] and ultra-wideband communication [8, 9]. However, wideband receivers are not only wideband to desired signals but also wideband to undesired interference.

[1]Z. Ru, N.A. Moseley, E.A.M. Klumperink, B. Nauta, "Digitally Enhanced Software-Defined Radio Receiver Robust to Out-of-Band Interference", IEEE Journal of Solid-State Circuits, vol. 44, no.12, pp. 3359–3375, Dec. 2009. © [2009] IEEE.

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5.1.1 Out-of-Band Interference (OBI) Problem and RF-Band Filters

Traditional wireless standards use dedicated fixed radio bands assigned by regulations, so that a clear distinction between in-band interference and out-of-band interference (OBI) exists. All transceivers should then comply to the wireless standard, and in-band interference can be mitigated via the standard (e.g. by forbidding adjacent channel use within the same cell). However, OBI is coming from "others" and can be much stronger. For popular mobile communication applications, in-band interference can be as strong as −30 to −20 dBm while the OBI can be as strong as −10 to 0 dBm [10]. An RF band-selection filter is then often employed to suppress OBI to below the in-band interference level. This requires an RF-filter with high quality factor and sharp roll-off. Usually these filters are not feasible on a CMOS chip and are implemented in a dedicated passive filter technology (e.g. surface acoustic wave (SAW) filters or more recently bulk acoustic wave (BAW) filters). Moreover, these are fixed-band filters with bands linked to the radio standards, i.e. they lack flexibility/programmability. Still, as any radio does, such an SDR aims at implementing selectivity. Now the desired band typically is the channel of interest and or a group of adjacent channels and we will call this "in-band". All interference outside the channel/band of interest can then be considered as OBI.

Without filtering, OBI can be very strong and we should worry about its effect on in-band signals. We can distinguish at least two mechanisms generating in-band distortion due to OBI (see Fig. 5.1):

1. Frequency translation of OBI via nonlinearity: e.g. intermodulation or cross-modulation
2. Frequency translation due to the time-variant transfer function of hard-switching mixers. Even for a perfectly linear circuit, time variance renders frequency shifts equal to the switching frequency and its multiples. This is often referred to as harmonic mixing, as harmonics of the "LO" mix OBI component on top of the desired signal, which is mixed down by the fundamental.

We will explain these two mechanisms briefly below and review state-of-the-art solutions for these problems.

5.1.2 Nonlinearity

As shown in Fig. 5.1a, nonlinearity can generate intermodulation and harmonic distortion products falling on top of the desired signal. Interference may also desensitize a receiver ("blocking") and produce cross-modulation [11]. It is easy to show that strong OBI poses a serious problem without filtering: a 0 dBm blocker in 50Ω corresponds to roughly $0.6\,V_{pp}$, so that two times voltage gain already clips OBI signals to a 1.2 V supply. Furthermore, IIP2 and IIP3 requirements

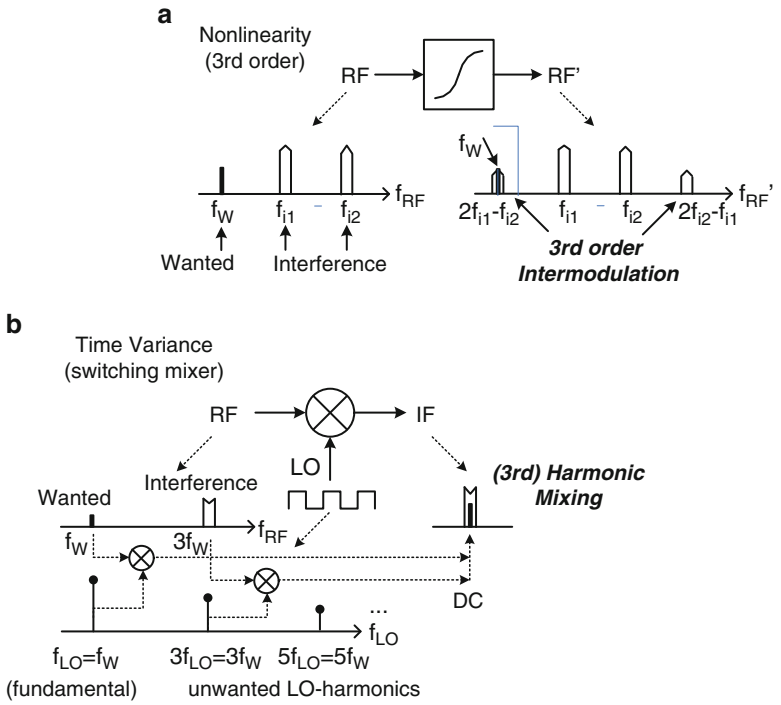

Fig. 5.1 Two basic mechanisms for frequency translation of OBI to in-band interference: (**a**) Nonlinearity (⇔ intermodulation, cross-modulation, e.g. IM3 distortion) (**b**) Time variance (⇔ harmonic mixing, aliasing, e.g. 3rd harmonic mixing)

become very tough without filtering, as exemplified in Table 5.1 for an example with 10 MHz receiver bandwidth and a noise figure of 4 dB (i.e. −100 dBm input referred noise floor). In [12] an overview of CMOS receivers published in the main solid-state circuits journals and conferences is given. For receivers operating in the communication bands up to 10 GHz, typically IIP3 values in the range of −20 dBm to 0 dBm are found, with a noise figure in the range of about 4–8 dB. In the overview [12], the "mixer-first architecture" [13] has the best IIP3 (+11 dBm) at 5–6 dB NF. Comparing to the values in Table 5.1, coping with input signals stronger than −30 dBm is problematic. Another issue that is sometimes neglected for wideband receiver is the "RF-to-RF" second order distortion [12], where two interfering RF signals render intermodulation at the sum or difference frequency (still at RF) which can interfere with the desired RF signal. For designs with a single ended input, not much higher values than IIP2 = +20 dBm are reported. Fully differential designs with IIP2 > 40 dBm have been reported, again allowing for a $P_{in,max}$ up to about −30 dBm (see Table 5.1).

One might wonder how the situation changes when we have knowledge about the OBI spectrum via spectrum sensing in a Cognitive Radio. We could then predict and

Table 5.1 Linearity and Harmonic Rejection requirements as a function of maximum input power level $P_{in,max}$ assuming no RF filtering, 10 MHz channel-bandwidth and 4 dB noise figure (i.e. −100 dBm noise floor)

$P_{in,max}$ (dBm)	IIP2 (dBm)	IIP3 (dBm)	P_1dB (dBm)	HR (dB)
−40	+20	−10	>−40	60
−30	+40	+5	>−30	70
−20	+60	+20	>−20	80
−10	+80	+35	>−10	90
0	+100	+50	>0	100

avoid channels polluted by intermodulation. However, analysis shows that cross-modulation effects easily push equivalent IIP3 requirements above +5 dBm [14].

Thus we clearly like to improve linearity. Two well-known techniques to do so are negative feedback and nonlinearity compensation. Negative feedback requires loop gain for linearization [15], which is not easily obtained at high frequencies. Also stability of the feedback loop is an issue and applying overall negative feedback to a complete receiver is non-trivial because of the frequency translation involved.

Nonlinearity compensation can work over a wide band but also has its limitations [16]:

1. Linearization often relies on two nonlinearity mechanisms that should compensate each other but don't automatically match, compromising robustness to process spread.
2. Linearization often relies on modeling of the weakly nonlinear region so that high IIP3 is only achieved for low 2-tone input power, with limited or lost benefit for strong interference.

Nonlinearity compensation has for instance been used in [17] and [18] in a Low Noise Amplifiers (LNA) to achieve an IIP3 in excess of +15 dBm. "Simultaneous Noise and distortion cancellation" [19–21] also is a form of nonlinearity compensation, but it only cancels the nonlinearity of the impedance matching device. Also, these techniques only address LNA linearity and not the succeeding stages such as mixer. Amplification pushes requirements on the linearity of a next-stage mixer, while the nonlinear output impedance of the LNA can also be a problem. Thus there is clearly room for further ideas to improve linearity and robustness to OBI.

5.1.3 Harmonic Mixing

As shown in Fig. 5.1b, linear time-variant behavior in a hard-switching mixer, or equivalently multiplication with a square wave, not only down converts the desired signal but also interference around LO harmonics. This harmonic mixing is of much less concern in narrowband receivers, relying on RF band-selection filters.

The 8-phase harmonic-rejection (HR) mixers as described in [22] can suppress RF signals around the 2nd to 6th LO-harmonics but amplitude and phase mismatches limit the achievable HR ratio typically to 30-to-40 dB [1, 23, 24]. However, as the last column in Table 5.1 shows, much more rejection is needed. If we want to bring harmonic responses down to the noise floor of −100 dBm, and cope with interferers of −40 to 0 dBm, a HR ratio of 60 to 100 dB is needed. State-of-the-art wideband TV tuners rely on RF tracking filters together with HR mixers [6, 7] to guarantee more than 65 dB HR ratio. However, these tracking filters can be power hungry and may degrade noise figure and linearity.

5.1.4 Contribution of this Chapter

As discussed above, OBI is problematic while dedicated RF filters are a flexibility bottleneck for SDR and CR. State-of-the-art multi-band receivers [25, 26] use multiple dedicated RF filters in parallel, increasing size and cost for every additional band. This chapter looks at ways to improve robustness to OBI in order to relax the requirements on RF filters or remove them altogether. Both analog and digitally-enhanced mixed-signal techniques are considered.

Both out-of-band nonlinearity and harmonic mixing can severely degrade signal-to-distortion ratio. Therefore, in our view a *practical SDR should not just be a wideband receiver, but also have enhanced out-of-band linearity and enhanced harmonic rejection*. This chapter presents an architecture improving IIP3 for OBI and the tolerance to out-of-band blockers (avoid compression). As will be explained later, this is achieved by exploiting a passive mixer in combination with the baseband filtering which can realize high-Q blocker filtering via frequency translated low-pass filtering. Moreover, to achieve high HR performance, two alternative HR techniques are presented: (1) a 2-stage polyphase HR technique implemented purely in the analog domain [27, 28]; (2) a mixed-signal technique exploiting digital adaptive interference cancelling (AIC) [29]. Both improve HR by rejecting harmonics in two successive steps (“iterative”), and both share the same 8-phase RF-to-baseband downconverter as a 1st HR stage. This chapter summarizes most of the work in [27–31]. Compared to [32], this work derives the interference estimate in another way and achieves better performance due to the better interference estimate. Also the work differs from our work on polyphase multipath transmitter [33–35], not only because we deal with a receiver instead of transmitter, but also in principle. In the transmitters we use equal and opposite phase shifts before and behind equal non-linear elements. Without any amplitude weighting this renders cancellation of harmonics and also many distortion components [33]. Here we use different weights and only a phase shift in the mixer clocks, only addressing harmonic rejection.

The rest of this chapter is organized as follows. Section 5.2 introduces a technique using low-pass filtering to mitigate blockers and improve out-of-band IIP3. Section 5.3 presents a 2-stage polyphase HR concept to improve amplitude accuracy obtaining high HR robust to mismatch. To improve both amplitude and

phase accuracy, a digitally-enhanced HR technique using AIC is presented in Sect. 5.4. The implementations of the analog front-end and the digital back-end are discussed in Sects. 5.5 and 5.6 respectively. Some key experimental results are presented in Sect. 5.7 with a comparison of analog and digital HR techniques as well as benchmarking to other work. The conclusions are drawn in Sect. 5.8.

5.2 Low-Pass Blocker Filtering

Traditionally, narrowband receiver front-ends use LNA-mixer combinations which can deliver sufficient linearity for in-band (IB) interference, typically IIP3 < 0 dBm, while an RF band-selection filter takes care of out-of-band (OB) interference. In SDR receivers, if OBI is much stronger than in-band interference, the required OB IIP3 is much higher than the required IB IIP3 and even desensitization can occur due to strong OB blockers. Therefore, frequency selective amplification or attenuation is desired. Tunable band-pass filtering (BPF) is in principle a solution, but it is difficult to provide sufficient selectivity and tunability simultaneously with good noise and linearity, using CMOS on-chip filters. Here we approach the problem from another angle.

5.2.1 Concept

To guarantee low NF, we need amplification early in the receiver chain. Voltage amplification in an LNA is usually realized via V-I conversion, often the transconductance of a transistor, followed by I-V conversion via some impedance or transimpedance. We can separate the two functional blocks, V-I and I-V, and insert a passive zero-IF mixer and a low-pass filter (LPF) in between, as shown in Fig. 5.2. The LPF drawn is conceptually current-in current-out, so ideally with no voltage swing. In practice, the functions of the LPF and the I-V conversion can be merged by using a frequency-dependent impedance, e.g. a parallel R and C.

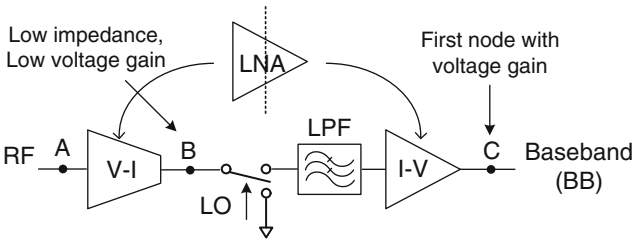

Fig. 5.2 Conceptual diagram of the low-pass blocker filtering

It is crucial to present a low impedance over a wide band to the output of V-I block, i.e. node B, so that little voltage gain occurs before filtering, leading to less distortion in the mixer and the nonlinear output impedance of the V-I block[1]. Therefore voltage gain occurs only at baseband after low-pass filtering, attenuating OBI products.

To quantify the blocker filtering effect, we may compare the 1dB compression point (P_{1dB}) for desired signals to the 1dB desensitization point (B_{1dB}) for blockers[2], both input referred. Assume a 3rd-order Taylor series for nonlinearity with α_1 and α_3 for the 1st and 3rd order coefficients respectively. Without any blocker filtering, it can be derived from [11] $P_{1dB} = 10 \cdot \log(0.145 \cdot |\alpha_1/\alpha_3|)$ and $B_{1dB} = 10 \cdot \log(0.0725 \cdot |\alpha_1/\alpha_3|)$. Therefore, B_{1dB} can be calculated based on P_{1dB}, and without blocker filtering, $B_{1dB} = (P_{1dB} - 3\,\mathrm{dB})$.

The LPF in Fig. 5.2 can mitigate blockers, and its bandwidth (BW) and order (n) determines the blocker filtering effect. If desensitization happens after I-V conversion, which is often the case due to a high voltage gain and limited voltage headroom, the suppression of blockers in dB by the LPF corresponds to the improvement of B_{1dB}.

However, for a wideband receiver the situation is more complicated, as one RF-blocker can be downconverted by different LO harmonics. For instance, a square-wave LO of 400 MHz converts a 1,250 MHz RF signal to 850 MHz and 50 MHz via the 1st and 3rd harmonic of the LO, respectively. The strongest downconverted signal depends on the blocker frequency (f_B) and the LO frequency (f_{LO}), i.e. which LO harmonic the blocker is closer to. Also it depends on the relative gain of the *m*th harmonic compared to the fundamental (1st) harmonic, i.e. the *m*th harmonic rejection ratio (HR_m).

Assume for simplicity that one blocker component dominates after downconversion and determines B_{1dB}. If $|f_B\text{-}m \cdot f_{LO}| \leq BW$, i.e. the blocker is within the LPF BW after downconversion by the *m*th harmonic, we find:

$$B_{1\mathrm{dB}} \approx (P_{1\mathrm{dB}} - 3dB) + \min\left[HR_m\right]. \tag{5.1}$$

If $|f_B\text{-}m \cdot f_{LO}| > BW$, i.e. the blocker is outside the LPF BW after downconversion by the mth harmonic, assuming an asymptotic filter characteristic, we find:

$$B_{1\mathrm{dB}} \approx (P_{1\mathrm{dB}} - 3dB) + \min\left[n \cdot 20\log\left(\frac{|f_B - m \cdot f_{LO}|}{BW}\right) + HR_m\right] \tag{5.2}$$

[1]Another motivation for low impedance at RF nodes is to widen the receiver's RF bandwidth as exploited in [8].

[2]P_{1dB} thus defines the (large) desired input signal power at which the receiver gain drops by 1dB ("1dB compression point", no blockers), while B_{1dB} defines the interfering single-tone blocker power for which the receiver gain for the (small) desired signal drops by 1dB.

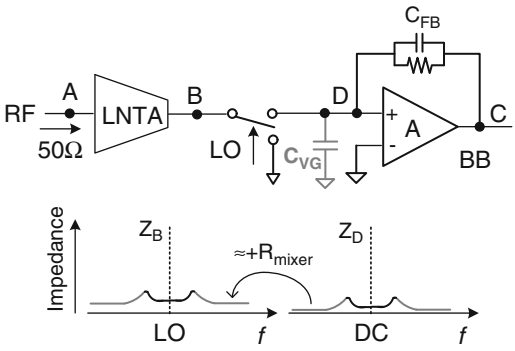

Fig. 5.3 Realization of the low-pass blocker filtering and illustration of impedance transfer effect

From (5.2) we can expect smaller bandwidth (BW) and higher order (n) of the LPF gives higher B_{1dB}, if f_B, f_{LO} and HR_m are fixed. Besides, we can also improve B_{1dB} by improving P_{1dB}. If compression happens at the receiver output, a lower receiver voltage gain or a larger output voltage headroom can improve the input referred P_{1dB}, and hence B_{1dB}.

The LPF can help to relax the OB linearity of the I-V conversion, however *not* for the V-I conversion. Therefore, the maximum achievable B_{1dB} is ultimately limited by the P_{1dB} of the V-I conversion minus 3dB. Thus linearity of the V-I conversion is very important and we will return to that point in Sect. 5.5. Via a similar mechanism, the OB IIP3 can also be enhanced compared to the IB IIP3.

5.2.2 Realization

A specific realization of the general concept (Fig. 5.2) is presented in Fig. 5.3. Zero-IF receivers commonly use an LNA with voltage gain followed by a V-I converter with current-mixer loaded by a LPF to suppress interference. We carry this approach one step further by entirely removing the voltage-gain LNA before the mixer and instead use a Low Noise Transconductance Amplifier (LNTA) as the first RF stage for the V-I conversion with input impedance matching. As mentioned before, maintaining a low impedance at node B over a wide band is important. This can be realized using low-ohmic switches in the passive mixers, while connecting their outputs to the virtual ground node of transimpedance amplifiers (TIA). The feedback network for the TIA consists of a parallel R and C to form a LPF. At high frequency, the feedback-loop gain drops so the virtual-ground impedance rises. By putting a capacitor C_{VG} to ground or across the differential virtual-ground nodes, the impedance at high frequency is reduced. Both C_{VG} and C_{FB} contribute to the total LPF function.

The bottom part of Fig. 5.3 shows, qualitatively, the impedance relationship between node B (Z_B) and node D (Z_D). Z_B is roughly equal to a scaled version of Z_D plus the mixer switch-on resistance (R_{mixer}), after frequency translation.

In contrast to active mixers, passive mixers don't have reverse isolation, so that the impedance behind the mixer at node D affects the RF-impedance seen from node B. Applying an RF current input, Appendix A [30] derives an estimate for Z_B for an N-phase mixer driven by 1/N-duty-cycle (non-overlapping) digital LO. Impedance Z_B at an RF frequency close to $m \cdot f_{LO}$ ($m = 1, 2, 3\ldots$), for an offset frequency $\Delta f(|\Delta f| \leq f_{LO}/2)$, can be written as:

$$Z_B(m \cdot f_{LO} + \Delta f) \approx R_{mixer} + \frac{N}{m^2 \cdot \pi^2} \cdot \sin^2\left(\frac{m \cdot \pi}{N}\right) \cdot Z_D(|\Delta f|), \tag{5.3}$$

Consider $m = 1$: for $N = 2$ or 4 the coefficient of Z_D is about 0.2, and for $N = 8$, it is about 0.12. For $m > 1$, the coefficient of Z_D is even smaller. As a result, unless very big switch transistors are used, R_{mixer} tends to play a dominant role in determining Z_B.

Besides delivering low impedance, this topology (Fig. 5.3) can also bring two other advantages exploited in some *narrowband* receivers [36–38]: (1) good *in-band* linearity in the I-V conversion due to the negative feedback; (2) low 1/f noise from the mixer switches working in the linear region which carry little DC current. In addition, this work [27] exploits this topology in a *wideband* receiver to enhance *out-of-band* linearity. Just a few months later, the idea has independently been proposed to realize SAW-less 3G receivers [39, 40]. If the LPF suppresses the OBI well, the main contributor to the OB nonlinearity will come from the V-I conversion of the LNTA, which can be quite linear as we will see later.

Although voltage amplification is avoided at RF, if the transconductance of LNTA is big, the receiver-input referred noise of the following stages, i.e. mixer and TIA, can be relatively small, so that the overall receiver NF can still be good and dominated by LNTA itself. As an example, the whole receiver in [38] achieves an NF of 2.2 dB based on a similar topology but in a narrowband configuration.

5.3 Two-Stage Polyphase Harmonic Rejection

The low-pass blocker filtering technique presented in the previous section acts after mixing, so it cannot prevent the harmonic mixing already occurring in the mixer stage. It is known that using a balanced LO can suppress all even-order harmonics. To also suppress odd-order harmonics, harmonic-rejection (HR) mixers using multi-phase square-wave LOs driving parallel operating mixers have been proposed before [22, 23]. Figure 5.4a shows an example, where the weighted current outputs add up to approximate mixing with a sine-wave LO. The combination of an amplitude ratio of $1{:}\sqrt{2}{:}1$ and an 8-phase LO (equidistant 45°) can reject the 3rd and 5th harmonics, as shown in the vector diagram of Fig. 5.4b. The 7th harmonic is not rejected and still needs to be removed by filtering, but the filter requirement is strongly relaxed compared to the case of a normal I/Q mixer whose first un-rejected harmonic is the 3rd order. However, the achievable HR ratio is limited by the accuracy of the amplitude ratios and the LO phases.

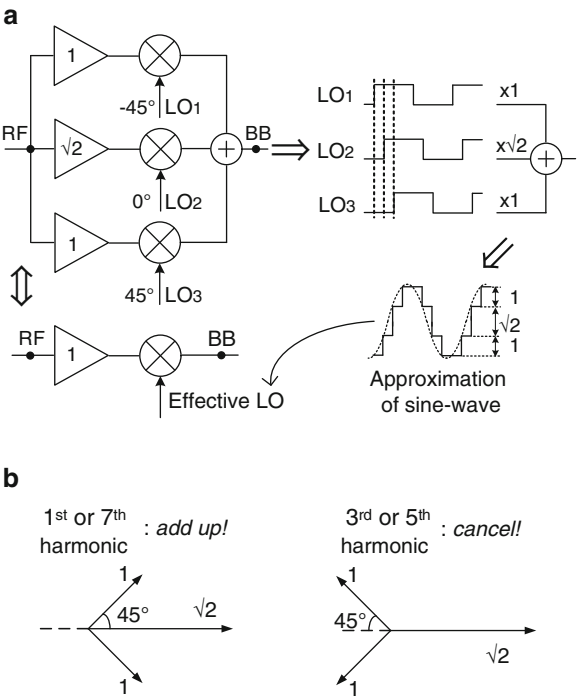

Fig. 5.4 (**a**) Block diagram of a traditional HR mixer; (**b**) its vector diagram

To achieve high HR ratio we need to accurately implement the desired weighting ratios, in this case the irrational ratio $1{:}\sqrt{2}$ accurately on chip. There are at least two challenges here: (1) realizing the right nominal (average) ratio; (2) keeping random variations due to mismatch small enough. To address these issues we propose a 2-stage polyphase HR concept (see Fig. 5.5) in which 2-stage *iterative* weighting and summing results in much higher HR than traditional HR mixers with only 1-stage. We will show that this iterative weighting results in a small product of relative errors for random variations, whereas the use of suitably chosen integer ratios results in sufficient accuracy to achieve a HR well above 60 dB.

5.3.1 Block Diagram

Figure 5.5 shows the block diagram of the 2-stage polyphase HR system, implemented on chip. The irrational ratio $1{:}\sqrt{2}{:}1$ is realized in two iterative steps with integer ratios: a first step with 2:3:2 and a second step with 5:7:5. The 1st-stage weighting is realized via 7 unit-LNTAs interconnected in 3 parallel groups to form the 2:3:2 ratio. The 2nd-stage weighting is realized via a baseband resistor network "R-net" between the TIA1 and TIA2 stages. The 5:7:5 amplitude ratio corresponds to the 7:5:7 resistance ratio, as the 2nd stage gain is inversely proportional to

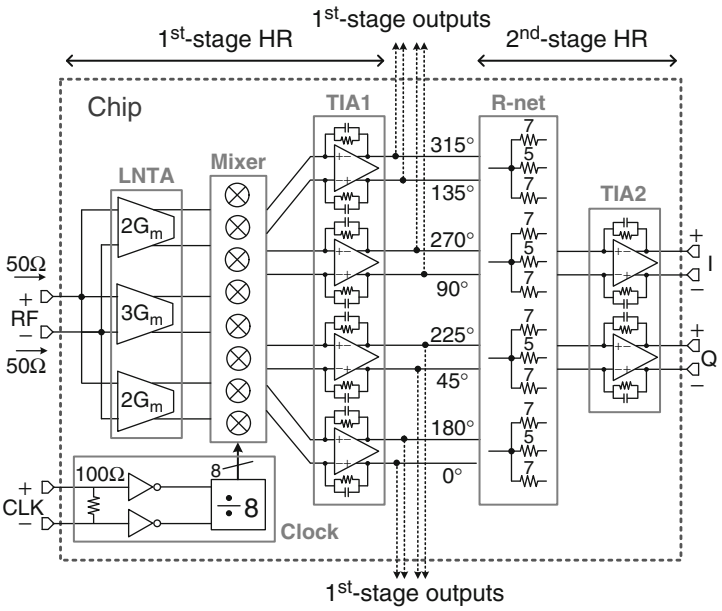

Fig. 5.5 Chip block diagram implementing the 2-stage polyphase HR and the low-pass blocker filtering

the resistors in the R-net block. The passive mixer array is driven by 8-phase 1/8-duty-cycle (non-overlapping) LO clocks. Via the combination of the LNTA, mixer and TIA with LPF, the first voltage gain occurs at baseband. Appendix B derives equations for the conversion gain of the receiver chain. Note that voltage gain occurs simultaneously with low pass filtering to achieve good OB linearity. Since harmonics can be as strong as blockers, it is important to have significant HR before the first voltage gain, especially because the anti-blocker filtering doesn't reduce harmonic images close to harmonics of the LO. The additional more accurate HR follows in the 2nd stage, aiming to bring residual harmonic images below the noise floor.

5.3.2 Working Principle

We will now show how we accurately approximate 1:$\sqrt{}$2:1 via 2:3:2 and 5:7:5. A key point is that the output of the TIA1 stage has 8 IF-outputs with equidistant phases, i.e. 0° to 315° with 45° step, instead of the conventional 4 phases, i.e. quadrature. This enables iterative HR by adding a 2nd stage. Figure 5.6 shows the weighting factor for the 8 outputs of the 1st-stage HR versus time (t) for one complete period of the LO (T). If we weight and sum three adjacent-phase outputs

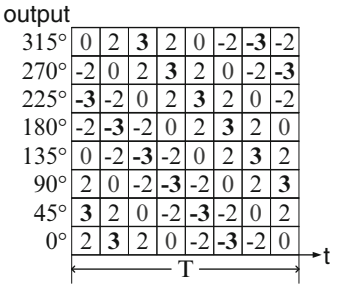

Fig. 5.6 Weighting factors for the 1st-stage HR outputs versus time

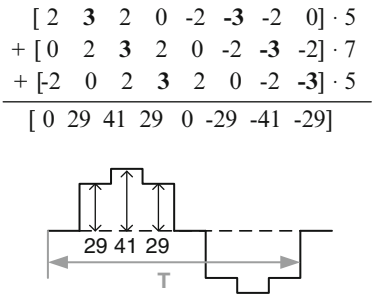

Fig. 5.7 Approximation of 1:$\sqrt{2}$:1 as 29:41:29 via integer ratios

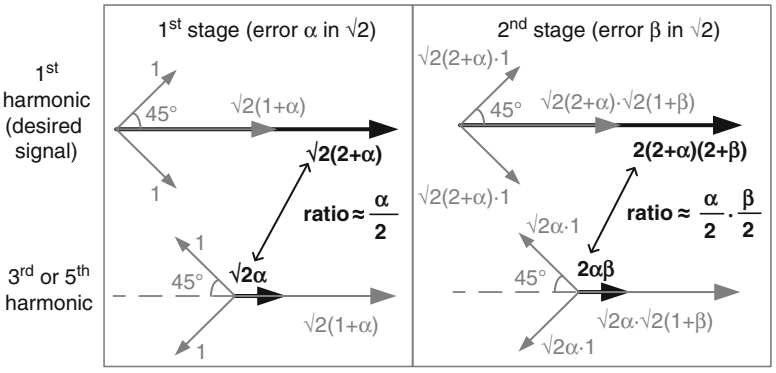

Fig. 5.8 Error reduction principle in the 2-stage polyphase HR (error $\alpha/2$ becomes a much smaller product of errors: $\alpha\beta/4$)

of the 1st-stage HR via the 2nd-stage weighting factors 5:7:5, as shown in Fig. 5.7, we find 29:41:29. The ratio 41:29 is equal to 1.4138, which represents only a 0.028% error from $\sqrt{2}$. This amplitude error corresponds to a HR ratio of more than 77 dB, if there is no phase error.

The 2-stage polyphase HR not only can approximate 1:$\sqrt{2}$:1 very closely, but it is also robust to amplitude mismatch, as illustrated in Fig. 5.8 via vector diagrams of the two stages. For the desired signal, polyphase contributions from three paths add

up, while for the 3rd and 5th harmonics, they cancel nominally. Assume now that the error in realizing $\sqrt{2}$ dominates and model it as a relative error α for the 1st stage and β for the 2nd stage. Also for simplicity, assume that the desired signal and the 3rd and 5th harmonics are equally strong at the receiver input and neglect the relative strength of different LO harmonics due to a certain LO duty cycle. After the 1st stage, the desired signal is multiplied by $\sqrt{2}\cdot(2+\alpha)$ and the 3rd and 5th harmonics by $\sqrt{2}\cdot\alpha$, leading to a relative error (interference-to-signal ratio) of $\alpha/2$ if $\alpha \ll 2$. For the second stage the same derivation holds. As the two stages are cascaded, the product of the gains determines the result, i.e. the total gain for the desired signal becomes $[\sqrt{2}\cdot(2+\alpha)]\cdot[\sqrt{2}\cdot(2+\beta)]$ and for the 3rd and 5th harmonics it is $[\sqrt{2}\cdot\alpha]\cdot[\sqrt{2}\cdot\beta]$. This renders a total relative error (interference-to-signal ratio) of

$$\frac{2\alpha\beta}{2\cdot(2+\alpha)\cdot(2+\beta)} \approx \frac{\alpha}{2}\cdot\frac{\beta}{2} \tag{5.4}$$

if $\alpha \ll 2$ and $\beta \ll 2$. Therefore, the total relative error is the *product* of the relative errors for the two stages, $\alpha/2$ and $\beta/2$. If the 2nd stage has an error $\beta = 1\%$, ideally this improves HR by $(\beta/2)^{-1}$, i.e. 46 dB, which has also been confirmed by simulation.

Please note that the product of errors, as shown in (5.4), holds for both 3rd and 5th harmonics. Moreover, it not just works for mismatch induced errors but for any amplitude errors, e.g. errors introduced by parasitic capacitance or finite LNTA output impedance.

Theoretically, more than two stages can achieve even better amplitude accuracy, but practically phase accuracy will often dominate. To also address the phase error, next we will propose an alternative HR concept that exploits digital techniques.

5.4 Digitally-Enhanced Harmonic Rejection

Even for the concept proposed in the previous section, the HR performance can still be limited by the amplitude and especially phase mismatches between the paths. In this section, we propose a digitally-enhanced HR architecture exploiting digital adaptive interference cancelling (AIC). Simply put, this concept adapts an estimate of the 3rd or 5th-order harmonic image in such a way that after subtraction from the received signal the HR ratio is increased.

The AIC concept is shown in Fig. 5.9: the interference estimate, v(n), is aligned in phase and amplitude with the interference in the received signal, r(n), by an adaptive digital equalizer. Thus, the equalizer removes the amplitude *and* phase differences of the interference between v(n) and r(n). The equalized interference estimate is subtracted from the received signal, which cancels the interference and produces the output signal, e(n).

Figure 5.10 shows a system-level block diagram of the proposed system. The analog front-end used is identical to the first stage of the 2-stage analog HR

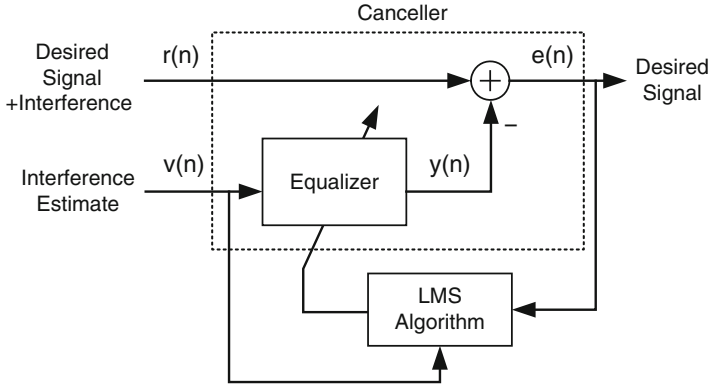

Fig. 5.9 A block diagram showing the concept of adaptive interference cancelling

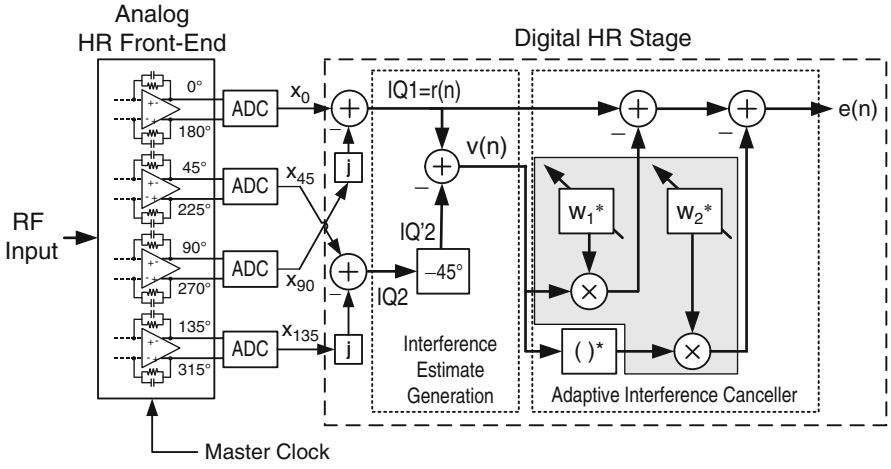

Fig. 5.10 A system-level block diagram of the analog front-end, the interference estimate generation and the AIC. The equalizer of the AIC is shown in grey

architecture proposed earlier. It produces four fully-differential signals, which are converted into the digital domain using four A/D converters, to form signals x_0, x_{45}, x_{90} and x_{135}. The HR of the analog down-mixer, typically in the range of 30–40 dB, relaxes the required dynamic range of the A/D converters.

Two complex-valued IQ pairs are formed using the four real-valued baseband signals:

$$\begin{aligned} \mathrm{IQ}_1(n) &= x_0(n) - j \cdot x_{90}(n) \\ \mathrm{IQ}_2(n) &= x_{45}(n) - j \cdot x_{135}(n) \end{aligned}, \tag{5.5}$$

where IQ_1 can be considered as the received signal and IQ_2 is an additional I/Q pair, needed to generate the interference estimate.

The baseband signals, x_0, x_{45}, x_{90} and x_{135}, are subject to analog component mismatches and LO timing errors, which cause amplitude and phase uncertainty. As a result, the amplitude and phase difference between the received signal, r(n), and the interference estimate, v(n), are subject to this uncertainty.

Perfect cancelling of the interference requires two conditions to be met: first, the interference estimate must be a perfect representation of the interference (i.e. it should not contain the desired signal) and second, potential amplitude and phase differences between the interference estimate and the actual interference must be completely removed by the equalizer.

Given the above, the equalizer must be adaptive to be able to cope with the uncertainty in the phase and amplitude in order to obtain the maximum amount of interference canceling. The equalizer consists of two single-tap FIR filters, which are formed by the complex coefficients, w_1, w_2 and the two associated multipliers shown in the grey portion of Fig. 5.10. The coefficients are adapted by applying the power-normalized LMS algorithm from [41].

For the single interferer case (only a 3rd or 5th-order harmonic image is present), the signal-to-interference ratio (SIR) of output e(n) after cancellation is determined by the inverse SIR of the interference estimate, v(n) [42]:

$$\mathrm{SIR}_{e(n)} \approx \frac{1}{\mathrm{SIR}_{v(n)}} \tag{5.6}$$

To maximize the SIR at the output of the canceller, the SIR of the interference estimate must be minimized. Therefore, the aim is to generate an interference estimate that contains the least amount of desired signal energy and the maximum amount of harmonic image energy.

5.4.1 Generating the Interference Estimate

The baseband outputs of the front-end, x_0, x_{45}, x_{90} and x_{135}, are formed by 8-phase 1/8-period-shifted LO waveforms that approximate a sinusoid, as explained in Sect. 5.3. An N/8-period time shift results in a $N \cdot 45^\circ$ phase shift for the desired signal and three & five times as much for the 3rd and 5th harmonic images[3]. This property is exploited in the generation of the interference estimate.

Considering only the relatively large (6%) approximation error of $1{:}\sqrt{2}{:}1$ by 2:3:2 (weighting ratio of the three LNTAs), the theoretical RF-to-baseband gain and rotation of the desired and 3rd & 5th-order signals are given in Table 5.2. For instance, the 3rd harmonic image is attenuated by $-20 \cdot \log_{10}(0.024) = 32.4\,\mathrm{dB}$, with respect to the desired signal.

[3]A time-shift is a linear phase operation. Thus, the resulting phase shift scales linearly with frequency.

Table 5.2 The RF-to-baseband transfer characteristics of IQ1, IQ2 and the interference estimate v(n), normalized to the desired signal

	IQ_1		IQ_2		Interference estimate, v(n)	
Signal	Gain	Phase	Gain	Phase	Gain	Phase
Desired	1.000	0°	1.000	45°	0.000	0°
3rd	0.024	−90.0°	0.024	135°	0.048	−90.0°
5th	0.014	90°	0.014	−45°	0.028	90.0°

The data for IQ_1 and IQ_2 in Table 5.2 can be derived using the mixer modeling technique used in [32], which uses the Fourier series of the effective LO waveforms and the LNTA weighting ratio. Note that the phase and amplitude relations between IQ_1 and IQ_2 are *independent of the actual RF signals*, i.e. modulation schemes.

By examining Table 5.2, it follows that the interference estimate, v(n), can be generated by a −45° rotation of IQ_2, which aligns the desired signal with respect to IQ_1. Subtracting the rotated IQ_2, i.e. IQ'_2, from IQ_1 cancels the desired signal but leaves the interference. Also other signal components in the interference estimate as shown in Table 5.2, can be derived using:

$$v(n) = \mathrm{IQ}_1(n) - \underbrace{\mathrm{IQ}_2(n) \cdot \exp\left(-j \cdot \pi \cdot \frac{45}{180}\right)}_{\mathrm{IQ}'_2(n)} \tag{5.7}$$

From Table 5.2 we can conclude that the 3rd harmonic image is attenuated by $-20 \cdot \log_{10}(0.048) = 26.4\,\mathrm{dB}$. This attenuation is solely due to the analog HR front-end and the application of (5.7). The 3rd harmonic image, in the interference estimate, is 6 dB stronger compared to IQ_1 or IQ_2 owing to a doubling of its amplitude by (5.7). This also holds for the 5th harmonic image. In addition, the desired signal is completely cancelled, despite the 6% error in $1{:}\sqrt{2}{:}1$. Thus, in theory, v(n) can be a good interference estimate.

5.4.2 The Adaptive Interference Canceller

In practical systems, the rejection of the desired signal in v(n) is limited by matching, just like the HR in the analog down-mixer. Fortunately, the AIC technique does not require perfect rejection of the desired signal to give good results. Consider a 3rd harmonic interferer and a desired signal that are equally strong after passing through the analog HR down-mixing stage. Given a realistic (matching limited) desired signal rejection of 40 dB during the interference estimate generation by way of (5.7), the SIR of the estimate, $\mathrm{SIR}_{\mathrm{v(n)}}$, is −40 dB. Using (5.6), the theoretical SIR after the AIC, $\mathrm{SIR}_{\mathrm{e(n)}}$, is 40 dB. Then the total harmonic rejection is 40 dB plus the rejection obtained by the analog 1st stage (typically in the range of 30–40 dB).

Given the above, it should be clear that the additional harmonic rejection provided by the AIC is dependent on the SIR of the baseband signals IQ_1 & IQ_2, which is equal to the signal-to-harmonic ratios of the RF antenna signal minus the HR of the analog front-end.

Interestingly, the performance of the AIC shows a favorable trend with respect to the interference power: if the interference power increases, the quality (1/SIR) of the interference estimate *increases*, which leads to an increased SIR at the output of the canceller. In practice, the benefit of this trend is limited by the nonlinearity of the front-end, including the A/D converters.

Consider again the block diagram of the digital HR stage in Fig. 5.10. The interference estimate, v(n), and its complex conjugate, $v^*(n)$, are equalized via multiplying by $w_1{}^*$ and $w_2{}^*$, respectively. The complex conjugate is needed to remove the I/Q imbalance image of the harmonic image in addition to the harmonic image itself [43]. The equalized signals are subtracted from the received signal, r(n), which removes the interference and produces the output signal, e(n). The filter weights, $w_1{}^*$ and $w_2{}^*$, are adapted with every new output value of e(n) by means of the LMS update rule [41]:

$$\begin{aligned} w_1(n+1) &= w_1(n) + \mu \cdot v(n) \cdot e^*(n) \\ w_2(n+1) &= w_2(n) + \mu \cdot v^*(n) \cdot e^*(n), \end{aligned} \tag{5.8}$$

where μ is the power-normalized step-size, normalized to the power of the interference estimate v(n), i.e. P_v:

$$\mu = \frac{1 \cdot 10^{-4}}{P_v} \tag{5.9}$$

and the canceller output, e(n), is calculated from the received signal, r(n), by:

$$e(n) = r(n) - w_1^*(n) \cdot v(n) - w_2^*(n) \cdot v^*(n), \tag{5.10}$$

as shown in Fig. 5.10.

The LMS update rule as in (5.8) is an iterative process that aims to minimize the cross-correlation between the output of the canceller, e(n), and the interference estimate, v(n). Cross-correlation is a measure of similarity, thus, minimizing it results in the output of the canceller being as *dissimilar* to the interference estimate as possible: the interference at the output, e(n), is reduced.

The choice of the step-size parameter μ in (5.9) is a tradeoff between speed and accuracy. Generally speaking, choosing μ too small results in slow convergence and choosing it too big increases the (time-varying) error of the filter weights [41], which reduces the harmonic rejection.

The optimum equalizer coefficients, w_1 and w_2, for cancelling the 3rd harmonic image may differ from the optimum coefficients for cancelling the 5th harmonic image, owing to different phase and amplitude mismatches for each image. The dominating interference largely determines the cross-correlation. Therefore, the dominating harmonic image, which normally is most problematic, will be cancelled by the AIC stage. Note that the preceding analog HR down-mixer stage rejects both images.

The optimum coefficients are independent of the RF signal modulation scheme, owing to the fact that the amplitude and phase *differences* between r(n) and v(n) are independent of the actual RF signals. Thus, once the filter coefficients to cancel a specific harmonic image have been found (by application of the iterative LMS algorithm), they remain valid until the mismatch introduced by the front-end changes, for instance, when making large changes in the LO frequency.

5.5 Implementation of the Analog Front-End

To verify the three concepts proposed in previous sections, an SDR receiver chip has been implemented in 65 nm CMOS. A detailed description of the chip design and measurements can be found in [27, 29–31]. Here we will only briefly describe aspects critically important for linearity and harmonic rejection. The digital AIC algorithm is realized in software and will be discussed later.

The block diagram of the chip has been shown in Fig. 5.5 and has been described in Sect. 5.3. The 8-phase LO is derived via a divide-by-8 from an off-chip signal CLK, i.e. the master clock. The receiver can be reconfigured to deliver either 8-phase outputs from TIA1 or I/Q outputs from TIA2. The 8-phase outputs interface to off-chip ADCs for digitally-enhanced HR measurements while the TIA2 stage is switched off. To better understand the implementation, we will describe the low-noise transconductance amplifier (LNTA), the clock generator, and the baseband blocks.

5.5.1 Linear Low-Noise Transconductance Amplifier (LNTA)

Figure 5.11 shows the schematic of a pseudo-differential unit-LNTA, of which there are 7 units in parallel to form three LNTAs with 2:3:2 ratio, sharing the same external (large-valued) inductor to GND for DC bias. The common-gate transistor M1 provides input impedance matching to 50 Ω, while the input is also capacitively coupled to transconductors implemented by inverters (e.g. M2 and M3). The total transconductance is in the order of 100 mS, where the inverters implement 80% and the common-gate matching stage 20%. A common-mode feedback (CMFB) loop using high-ohmic resistors and an amplifier "A" controls the PMOS transistors and ensures all three LNTA outputs are biased around half the supply voltage.

Since the LPF improves the OB linearity of I-V conversion (Fig. 5.2), the V-I linearity sets the ultimate limit of OB linearity. To obtain a good V-I linearity, high $(V_{GS} - V_{TH})$ and high V_{DS} is desired. In our VDD = 1.2 V design, $(V_{GS} - V_{TH})$ of 65 nm transistors is larger than 250 mV and V_{DS} is 600 mV. Simulations predict an IIP3 of more than +15 dBm for a load resistance <100 Ω and only ±1 dB variation over different process corners, indicating that high LNTA linearity robust to process spread is possible if we keep voltage gain low (small R_L) (see [31] for more details on linearity optimization).

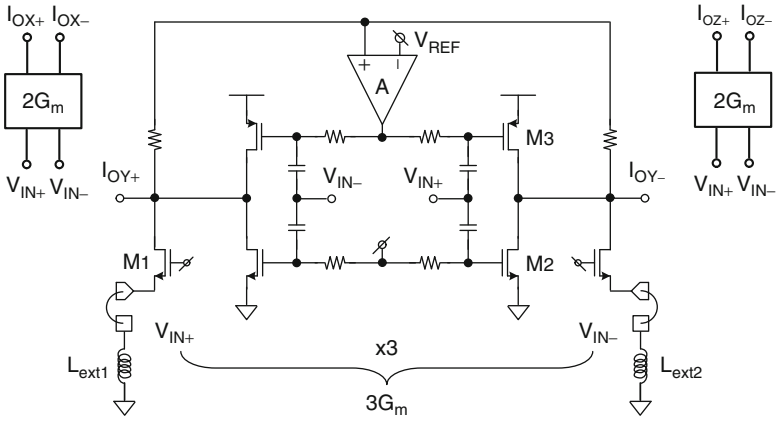

Fig. 5.11 Low Noise Transconductance Amplifiers (LNTA) implementing $3G_m$ (shown on transistor level) and two blocks of $2G_m$ (identical schematic)

A differential LNTA requires an off-chip balun if a single-ended antenna or RF filter is used. Compared to an LNTA with single-ended input, although the differential one may double the power consumption [44], it can render better IIP2. Besides, the input voltage swing on each of the differential inputs is lowered by 3 dB, which improves LNTA IIP3 and P_{1dB} by 3 dB.

5.5.2 *Accurate Multiphase Clock*

Since the amplitude accuracy can be ensured by the 2-stage polyphase HR, the phase inaccuracy is likely to dominate. Based on Appendix B, if the LO duty cycle is "d", the resulting 3rd HR (1σ) is

$$HR3 = 10\log\left(\frac{\sin^2(\pi\cdot d)}{\sin^2(3\pi\cdot d)}\cdot\left[\left(\frac{\sigma_A}{12}\right)^2+\left(\frac{\sigma_\varphi}{4}\right)^2\right]^{-1}\right), \tag{5.11}$$

where σ_A and σ_φ are the standard deviation in the amplitude and phase respectively. For $d = 1/8$ and negligible amplitude error $(\sigma_A \to 0)$ due to the 2-stage technique as in (5.4), to reach 60 dB HR (3σ), the required phase error is $\sigma_\varphi = 0.03°$.

To build a multiphase clock generator with low phase mismatch, two design principles are applied: (1) to use a common master clock to derive all phases; (2) to minimize the path from the common master clock to the mixer switches therefore to minimize mismatch accumulation.

Figure 5.12 shows a divide-by-8 ring counter using eight dynamic transmission-gate (TG) flip-flops (FF). The same master clock (CLK), with 8-times the LO frequency, drives all FFs. Only one inverter (INV2) is used as a buffer to minimize the path from CLK to mixer.

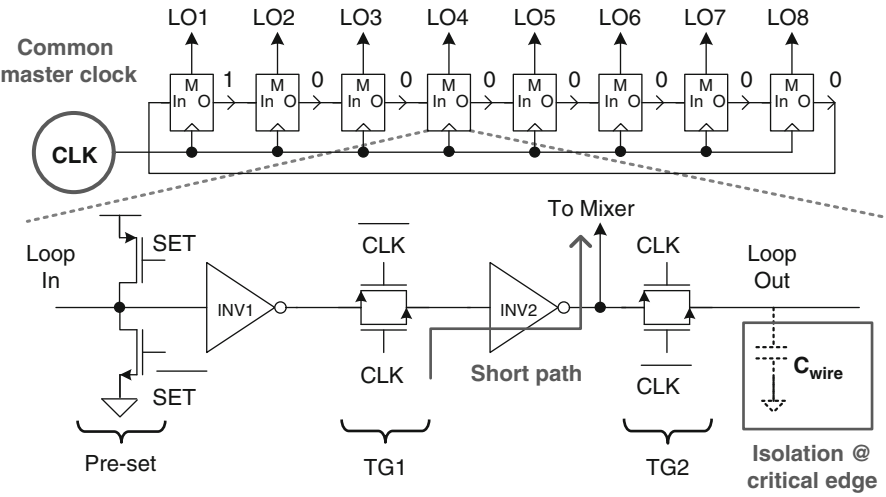

Fig. 5.12 An 8-phase clock generator with low phase mismatch (with one cell shown on transistor level)

A preset data pattern is required to deliver the wanted 1/8 duty cycle. Each LO phase controls 6 mixer switches connecting to differential outputs of three LNTAs. The gates of all the 6 switches are connected together and driven by the same buffer, i.e. INV2, to minimize buffer mismatch.

In a ring counter, all flip-flops "see" the same environment. However, a loop is not convenient in layout and it may need different wiring lengths between each two flip-flops, degrading phase accuracy. A careful layout strategy is adopted to minimize the wiring differences. Moreover, when the critical LO edges occur, the largest part of the wiring is isolated from the output of INV2 via TG2, decreasing rise and fall times and reducing the effect of wiring mismatch.

Figure 5.13 presents the simulated phase deviation from 45° between two adjacent 0.8 GHz LO phases due to mismatch, including the contribution from mixer switches. The histogram shows a maximum phase error of only 0.07° and it yields $\sigma = 0.024°$, i.e. 0.08 ps for 0.8 GHz. This clock performance is hence compatible with HR $>$ 60 dB (3σ).

The master clock CLK comes from an off-chip generator followed by a pair of inverters as on-chip buffer. Simulation shows, at 0.8 GHz LO, the power consumption of the divider is 5.4 mA at 1.2 V supply and the input buffers consume 8.9 mA driven by 6.4 GHz differential input clock.

5.5.3 High-Swing TIA and Baseband R-Net

Since the voltage gain occurs at the outputs of the TIA1 stage where interference is only partly suppressed, we choose an OTA topology [30] which can handle large

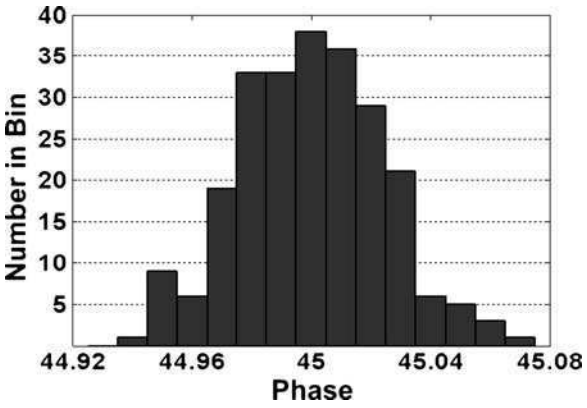

Fig. 5.13 Histogram of the simulated phase difference between two adjacent LO outputs (240 Monte Carlo results)

voltage swing, aiming to tolerate large blockers. It is a two-stage class-AB-output OTA based on [45] and its schematic can be found in [30]. The input pair uses NMOS transistors in weak inversion for high g_m/I_{DC} and a big size leading to low 1/f noise. For the OTA second stage, a class-AB push-pull output stage is used, which can handle more than 2 V peak-to-peak differential output voltage swing. Each OTA draws 3 mA from 1.2 V supply.

A parallel RC feedback network implements a simple 1st-order LPF to perform blocker filtering (Fig. 5.5). Each TIA stage has a LPF −3 dB bandwidth of 20 MHz and together they determine the receiver IF bandwidth of 12 MHz, which may accommodate most mobile communication standards. The virtual-ground impedance of the TIAs is about 4 Ω around DC and peaks to 60 Ω around 700 MHz. The simulated gain after the TIA1 stage is 27 dB and after the TIA2 stage 34 dB.

The resistor network (R-net) provides the 2nd-stage weighting for HR. It also converts 8-phase outputs of the TIA1 stage into quadrature inputs of the TIA2 stage. To form a 5:7:5 amplitude ratio, 19 unit-resistors form a resistance ratio of 7:5:7 in 3 paths. Harmonic rejection at baseband (via R-net) can also reduce errors due to parasitic capacitance compared to at high frequency.

5.6 Implementation of the Digital Back-End

The analog front-end used in the digitally-enhanced HR architecture consists of the 1st stage HR mixer driven by the multi-phase clock generator of the 2-stage analog HR architecture. The four fully-differential baseband outputs provided by the TIA1 stage (Fig. 5.5) are converted into the digital domain using a commercial A/D board comprising four 14-bit ADCs (Fig. 5.10). Unfortunately, the input range of the used A/D board was more than 15 times greater than the output swing provided by the front-end, resulting in less than 10 effective bits.

The baseband processing, including the interference estimate generation and the adaptive interference canceller were implemented in software on a PC and use

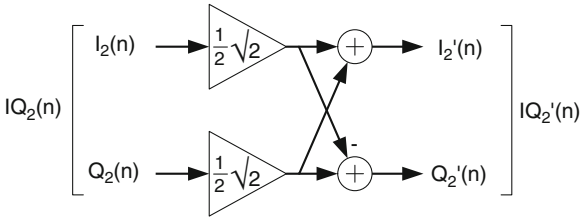

Fig. 5.14 Reduced complexity −45° phase shifter

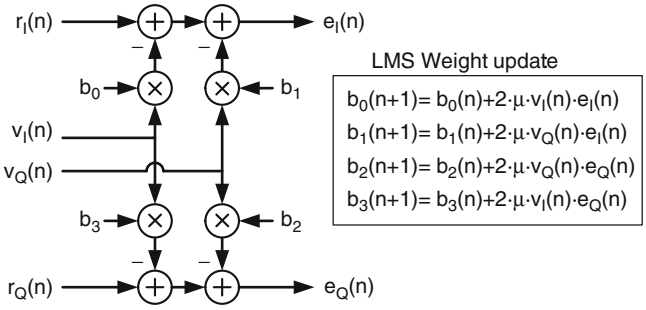

Fig. 5.15 Reduced complexity interference canceller

floating-point arithmetic. To allow real-time processing, a sampling rate of 4MS/s was chosen. This gives 2 MHz bandwidth for each analog baseband signal and 4 MHz bandwidth in the digital domain using quadrature signals. Figure 5.10 gives a system-level overview of the setup.

The interference estimate generation is implemented using 2 real adders and the phase shifter, shown in Fig. 5.14. This reduced-complexity shifter exploits the fact that the cosine and sine of a 45° angle are of equal magnitude. Thus, it needs 2 real multipliers (instead of 4) and 2 real adders. Thus, the total complexity of the interference estimate generation is 2 real multipliers and 4 real adders.

The complexity of the canceller indicated by (5.10) can be reduced from 8 multipliers and 8 adders to 4 multipliers and 4 adders, by applying the following substitutions:

$$\begin{aligned} b_0 &= w_{1,I} + w_{2,I} \qquad b_1 = w_{1,Q} - w_{2,Q} \\ b_2 &= w_{1,I} - w_{2,I} \qquad b_3 = -w_{1,Q} - w_{2,Q} \end{aligned}, \tag{5.12}$$

where the filter coefficients, w_1 and w_2, are split in their real and imaginary parts, $w_{1,I}$, $w_{1,Q}$, etc. The resulting canceller and the new LMS weight update rules are shown in Fig. 5.15. If the step-size μ is rounded to the nearest power of two, 4 multipliers in the "LMS Weight update" become a shift operation. As a result, the update mechanism only needs 4 multipliers and 4 adders. Then, the total arithmetic complexity of the digital HR stage is 10 multiplications and 12 additions per sample.

While the digital algorithm was implemented only in software, a fixed-point VHDL version was synthesized using a 65 nm CMOS standard cell library. The tools reported a dynamic power of less than 10 mW at 100 MS/s and 1.2 V supply voltage.

5.7 Experimental Results

The circuit shown in Fig. 5.5 is fabricated in 65 nm CMOS and the micrograph is shown in Fig. 5.16. The total area, excluding bond-pads, is about 1 mm^2. Capacitors (C_{FB} and C_{VG} in Fig. 5.3) take a large portion of area in the TIA, and also the OTA input pair is big to achieve a low 1/f noise corner. With 1.2 V supply, the analog power consumption is 33 mA (LNTA: 14 mA, TIA1-stage: 12.8 mA, TIA2-stage: 6.4 mA) while the clock power consumption is 8 mA at 0.4 GHz LO and 17 mA at 0.9 GHz LO, including the clock input buffers.

To prove the receiver is robust to OBI, all measurements are performed on PCB without any external filter. Two SMD inductors are mounted on the PCB to bias the LNTA (Fig. 5.11). Both the receiver inputs and clock inputs are differential and wideband hybrids (balun) were used to interface to single-ended 50Ω measurement equipments. The IF-output voltages are sensed by a differential active probe that performs differential to single-ended conversion and impedance conversion to 50Ω. The characteristics of all components and cables for testing are de-embedded from the results.

The divide-by-8 works up to 0.9 GHz LO, and the measured S_{11} is lower than −10 dB up to 5.5 GHz. This means the HR measurement is valid for 0.9 GHz LO up to its 6th harmonic. The measured IF bandwidth is 12 MHz and the baseband 1/f noise corner is 30 kHz thanks to the passive mixer with little DC current and the OTA with a large-sized input pair.

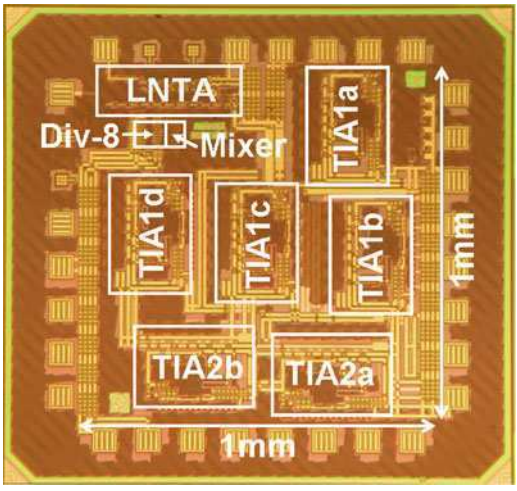

Fig. 5.16 Micrograph of the 65 nm-CMOS chip indicating some functional blocks

5.7.1 Gain, NF, RF Bandwidth, and In-Band IIP2/IIP3

The voltage gain and DSB NF were measured over an LO frequency of 0.4–0.9 GHz. The voltage conversion gain, measured for an IF of 1MHz from the input of the balun to the differential outputs of receiver, is above 34 dB over the whole band and is quite flat (±0.2 dB variation), indicating a much wider RF bandwidth. The NF is measured for an IF of 10MHz since the available NF analyzer (Agilent N8973A) starts from that frequency. The DSB NF is below 4 dB except for 0.4 GHz where 1/f noise from the LNTA starts to dominate.

The divide-by-8 limits the LO frequency range up to 0.9 GHz (master clock @ 7.2 GHz), but the signal-path −3 dB RF bandwidth is much wider, up to 6 GHz. To verify it, we conducted a gain measurement for the 7th harmonic, i.e. the first non-canceled high-order harmonic. Ideally, using 1/8 duty-cycle LO, the strength of the 7th harmonic should be 1/7 of the fundamental harmonic, so we expect the 7th harmonic should ideally have a gain that is 16.9 dB (1/7) lower from 34 dB, i.e. 17.1 dB. Indeed, the gain drops from 17 dB at 0.7 GHz RF to 14.3 dB at 6 GHz RF (LO: 0.1 to 0.85 GHz), which means the OBI will only be attenuated a little by the frequency roll-off at RF.

In-band IIP2 and IIP3 were also measured and are rather insensitive to LO frequency over the 0.4–0.9 GHz band. Two tones close to the LO frequency were used, so that they are not affected by IF filtering (IIP2: $f_{LO} + 3$ MHz and $f_{LO} + 6.01$ MHz; IIP3: $f_{LO} + 3$ MHz and $f_{LO} + 3.01$ MHz). After downconversion, the IM2 component at 3.01 MHz and the IM3 component at 2.99 MHz are measured. The IB IIP3 is around +3.5 dBm, which is good given the high gain of 34 dB, thanks to only voltage gain at baseband with negative feedback. The IB IIP2 is above +46 dBm.

5.7.2 Out-of-Band IIP2/IIP3

We also measured the out-of-band (OB) IIP2 and IIP3. Due to the LPF behavior, the measured OB linearity depends on the distance from f_{LO} to the two RF tones used. For sufficient distance, the LPF will suppress the downconverted two-tone interference so the OB nonlinearity is mainly contributed by the V-I of the LNTA.

The OB IIP3 is tested via two tones at 1.61 GHz and 2.40 GHz with an LO at 819 MHz, so that the IM3 is at 820 MHz RF and 1 MHz IF. Without fine tuning, the measured OB IIP3 is +16 dBm, which agrees with the simulated results. Compared to the IB IIP3 of +3.5 dBm, the OB IIP3 is dramatically improved because the TIA was dominating the IB IIP3, due to the high voltage gain at the output. The OB IIP2 is +56 dBm, tested via two tones at 1.80 GHz and 2.40 GHz while LO at 601 MHz, so that the IM2 is at 600 MHz RF and 1MHz IF.

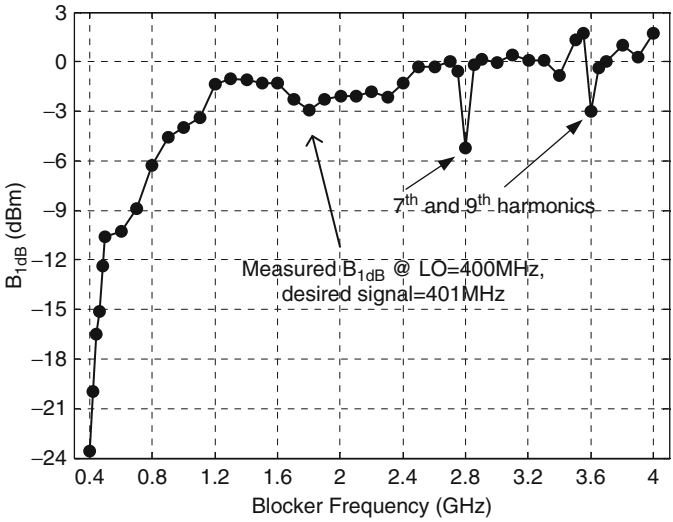

Fig. 5.17 Measured input-referred 1 dB desensitization point (B_{1dB}) versus blocker frequency

5.7.3 One dB Compression Point and Blocker Filtering

To quantify the effect of the blocker filtering, we measured the 1 dB compression point (P_{1dB}) and the 1 dB desensitization point (B_{1dB}), both input referred. First we measured the P_{1dB} without applying any blockers, which is -22 dBm. The result is reasonable since -22 dBm input power plus 34 dB voltage gain corresponds to a single-ended opamp output voltage swing of about 1.27 V peak to peak, just exceeding the 1.2 V supply. This means the compression limitation is at the receiver output and the P_{1dB} can be improved by automatic gain control (AGC).

A more serious problem is to receive a weak signal at the same time with a strong interferer: a so-called blocker test. In this situation AGC doesn't help since the maximum gain is required to maintain sensitivity. The measurement was carried out with the LO at 400 MHz and the desired RF signal at 401 MHz with -50 dBm input power. The blocker frequency is varied from 402 MHz to 4.002 GHz. Figure 5.17 shows B_{1dB} versus the blocker frequency. As predicted by (1) and (2), we see two effects in the figure: (1) the tolerable blocker power depends on the frequency distance between the LO and the blocker, due to the LPF behavior[4]; (2) HR also plays a role in blocker filtering, as two dips occur around 7th and 9th harmonic of the LO frequency, both of which are not rejected well by the 8-phase HR. From the figure, we can observe that B_{1dB} is better than P_{1dB} $(-22\,\text{dBm})$ except very close-by blockers (402 MHz) and the maximum B_{1dB} is more than 0 dBm, showing the blocker filtering is indeed effective.

[4]The actual behavior of the LPF is more complicated than (5.2), since our baseband filter is cascaded in two stages, which does not follow a simple 1st-order or 2nd-order filtering behavior.

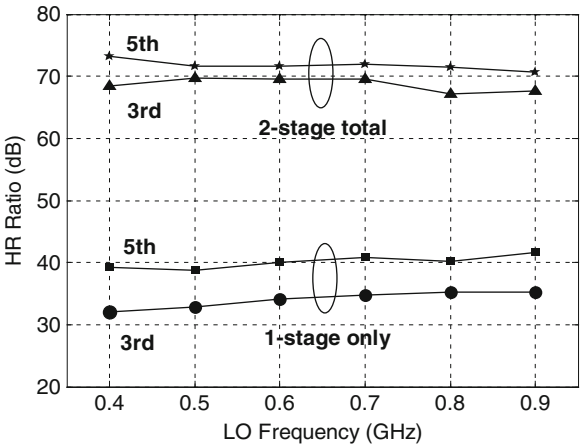

Fig. 5.18 Measured HR ratio versus LO frequency: comparison between HR with only 1-stage and total 2-stage (2-stage polyphase HR)

5.7.4 Two-Stage Polyphase HR

We will verify the analog 2-stage polyphase HR here and later the digitally-enhanced HR. Afterwards, these two alternative approaches will be compared.

First we look at the 2-stage polyphase HR. The HR ratio can be measured by comparing the gain difference between the desired signal and the harmonic image. At the receiver input, the desired signal power was −50 dBm while the harmonic image power was −30 dBm.

Figure 5.18 shows the HR of the first stage, at the outputs of the TIA1, and the total 2-stage HR, at the outputs of the TIA2, versus LO frequency. The 1-stage HR is between 30 and 40 dB and the 2-stage HR is around 70 dB, representing a 30 dB improvement for both 3rd and 5th HR thanks to the 2-stage polyphase HR technique. Generally, the HR improvement from 1-stage to 2-stage is in the range of 20 to 40 dB, observed from measuring multiple chips. As the 2-stage technique mainly reduces the amplitude error, the large improvement also indicates that it is the amplitude error dominating the 1st-stage HR.

To identify the effect of mismatch, we measured the 2-stage HR for 40 chips at 0.8 GHz LO, as shown in Fig. 5.19. The minimum 3rd order HR is 60 dB and the minimum 5th order HR is 64 dB. The 2nd, 4th, and 6th HR is also measured, over 20 chips. The minimum 2nd-order HR is 62 dB, while the minimum 4th and 6th order HR are both 67 dB. These results are achieved without calibration, trimming, or RF filtering.

Since the signal-path −3 dB RF bandwidth has been characterized to be up to 6 GHz, the contribution of the frequency roll-off to the HR result should be small. According to (5.11), the simulated phase error $\sigma = 0.024^\circ$ means a minimum HR (3σ) of 62 dB if the amplitude error is eliminated, fitting well with the measured HR as well as the Monte Carlo simulation results. This also suggests that phase error can be the limitation now.

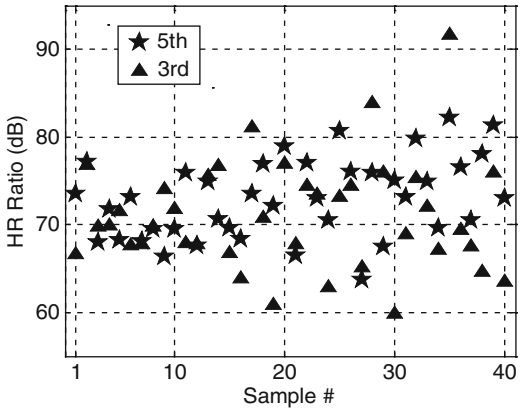

Fig. 5.19 Measured HR ratio of 40 randomly-selected chips at 800 MHz LO (2-stage polyphase HR)

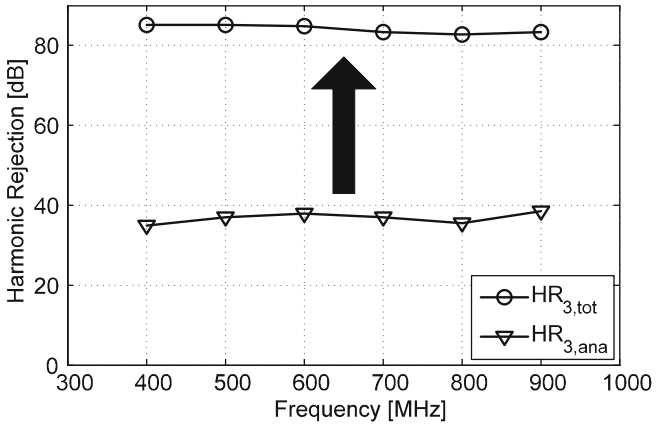

Fig. 5.20 The measured 3rd-order HR of the analog stage and the combined stages versus the LO frequency. Desired: −66.1 dBm RF power, 3rd harmonic image: −20.1 dBm RF power (digitally-enhanced HR)

5.7.5 Digitally-Enhanced HR

Consider now the digitally-enhanced HR architecture. The harmonic rejection for the 3rd harmonic image versus LO tuning range (0.4–0.9 GHz) was measured, see Fig. 5.20. At the receiver input, the desired signal RF power was −66.1 dBm and the harmonic image RF power was −20.1 dBm. The analog HR mixer provides more than 36 dB HR for the 3rd harmonic image, which is higher than the 32.4 dB predicted by Table 5.2. We attribute this difference to the finite output impedance of the three LNTAs. Thus, the effective weighting of the 2:3:2 ratio is closer to the ideal $1{:}\sqrt{2}{:}1$, resulting in a higher measured HR.

Given a SIR of −46 dB at RF, the digital AIC increases the harmonic rejection provided by the analog HR mixer from 36 dB to over 80 dB across the entire LO

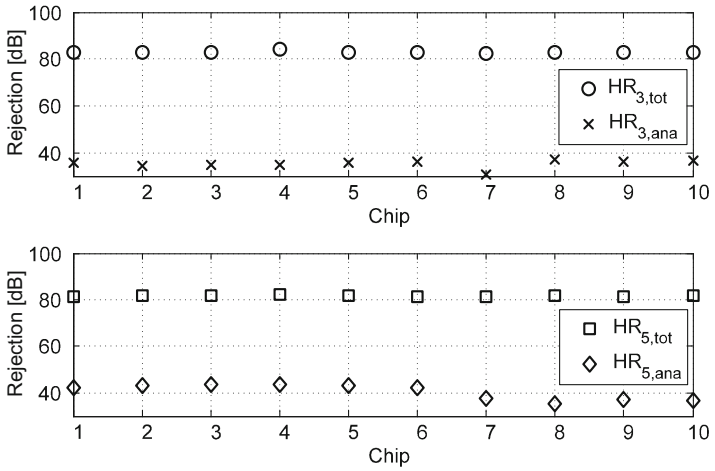

Fig. 5.21 The measured 3rd and 5th-order HR of the analog stage and combined stages, for 10 randomly-selected chips, at 800 MHz LO (digitally-enhanced HR)

tuning range. The HR measurements are calculated based on the difference in power between the desired signal and the harmonic image. At the output of the digital canceller, the harmonic image is below the noise floor. Instead of the harmonic image power, the noise floor was taken. Thus, the actual HR is greater than what is shown in Fig. 5.20.

A second indicator that the HR is higher comes from the SIR of the interference estimate, v(n), which was measured to be over 52 dB (limited by noise floor of equipment) across the entire LO tuning range. Given (5.6), the (theoretical) SIR at the output of the canceller is also 52 dB. The power ratio between the desired signal and the harmonic image (at RF) is −46 dB, which makes the theoretical HR greater than 98 dB! Unfortunately, the height of the noise floor at the output of the canceller, which is largely determined by the quantization noise of the A/D board, prevents this to be verified.

The 3rd and 5th-order harmonic rejection for multiple (randomly selected) chips is shown in Fig. 5.21. The desired signal RF power was −66.1 dBm at 800 MHz LO. The RF power of the 3rd and 5th-order harmonic images was −20.1 dBm. The results show more than 36 dB of analog harmonic rejection and more than 80 dB of combined harmonic rejection, for all chips. Thus, the digitally-enhanced AIC technique performs well under varying mismatch conditions.

5.7.6 Comparing the Alternatives

Table 5.3 summarizes the main properties of the two alternative approaches. The 2-stage polyphase HR implemented in analog approach helps both 3rd and 5th HR

Table 5.3 Comparison of two alternative HR techniques robust to mismatch

	Analog 2-stage	Digital A|C
Rej. strongest	>60 dB	>80 dB[a]
Rej. other odd	>64 dB	>36 dB
Rej. even	>62 dB	>64 dB
Power front-end	50 mA @ 1.2V (excl. ADCs)	44 mA @ 1.2V (excl. ADCs)
Power DSP (100 Msps)	N/A	<8.5 mA @ 1.2V (simulated)
#ADCs	2	4

[a]If one harmonic interference image band is dominating

via improved amplitude accuracy and achieves a minimum rejection of 60 dB and 64 dB respectively. The digitally-enhanced HR based on AIC algorithm consistently shows more than 80 dB of HR for a single harmonic image (either the 3rd or the 5th) by correcting both amplitude and phase of that harmonic image. The other harmonic image is rejected by at least 36 dB, not improved from the analog 1st stage. They share a similar limitation on even-order HR.

On the implementation level, compared to the 2-stage polyphase HR, the digitally-enhanced HR architecture requires two additional A/D converters, which may increase the power considerably. Fortunately, the converters for x_{45} and x_{135} (Fig. 5.10) may be switched off when the analog HR stages can provide enough harmonic rejection.

5.7.7 Performance Summary and Benchmark

In [31] the design was benchmarked to other published wideband receivers with HR, showing competitive linearity and much higher harmonic rejection. Comparing all work including an LNA, [1, 7, 46] shows an IIP3 around −15 dBm while this work shows an IIP3 of +3.5 dBm and a competitive NF. The OB IIP3 of our work is even higher (+16 dBm), but we didn't find a good way to benchmark it. For HR, only [46] and [47] reported numbers comparable to this work. However, Maxim et al. [47] only reported results from one chip while consuming large power due to a different structure of the HR mixer. Hyouk-Kyu et al. [46] reported results for 10 chips, but relying on hand calibration, and the calibration is only effective for either 3rd or 5th HR but not for both at the same time. Thus we conclude that our design has both good linearity and good HR at moderate power consumption, thanks to the proposed techniques.

5.8 Conclusions

This chapter identified out-of-band (OB) nonlinearity and harmonic mixing as two main problems for *out-of-band interference* (OBI), and proposed solutions to reduce their effects. First, OB nonlinearity can be improved by implementing

low-pass filtering, simultaneously with voltage gain only after downconversion. Moreover, using passive mixers, the low-pass impedance in baseband is frequency translated to a high-Q RF-band filter around the LO-frequency, further attenuating blockers. These techniques improve the OB IIP3 and the desensitization point due to blockers. Second, two "iterative" harmonic-rejection (HR) techniques are presented to reduce harmonic mixing in a way which is robust to mismatch. An analog 2-stage polyphase HR concept is proposed to greatly enhance the amplitude accuracy for both 3rd and 5th harmonics so that the total amplitude error becomes product of errors. Alternatively, digitally-enhanced HR based on adaptive interference cancelling (AIC) can be applied to improve HR of the analog 1st-stage further by correcting both amplitude and phase errors for one dominant harmonic, either 3rd or 5th. To guarantee a mismatch-robust HR for both analog and digital approaches, a simple but accurate ring counter is presented to generate the multiphase clocks driving the HR mixer.

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Appendices

A. Mixer Input Impedance Derivation

This appendix derives (5.3) for the mixer in Fig. 5.22, consisting of N switches in parallel driven by N-phase non-overlapping LO-clock signals, each with $1/N$-duty-cycle. Thus there is always one current path via one impedance Z_{BB} and switching results in frequency shifting of RF current $i_{src}(f_{RF})$. For $f_{RF} \geq 0$ this renders baseband signals across Z_{BB} of the form:

$$v_{BB}(f_{RF} - m \cdot f_{LO}) = H(-m) \cdot i_{src}(f_{RF}) \cdot Z_{BB}(f_{RF} - m \cdot f_{LO}). \tag{5.13}$$

Where $H(-m)$ is the Fourier coefficient associated with the frequency shift $-mf_{LO}$ related to the (m)th LO harmonic. For a $1/N$-duty-cycle square-wave LO with a delay of t_0, the Fourier coefficients are:

$$H(m)|_{m\neq 0} = \frac{1}{m \cdot \pi} \cdot \sin\left(\frac{m \cdot \pi}{N}\right) \cdot e^{-j \cdot m \cdot 2\pi \cdot \frac{t_0}{T}}, H(0) = \frac{1}{N}. \tag{5.14}$$

After filtering in baseband, this baseband voltage is upconverted to v_{RF} again, resulting in a contribution at f_{RF} by the mth LO-harmonic which can be written as:

$$v_{RF}(f_{RF}) = N \cdot H(-m) \cdot H(m) \cdot i_{src}(f_{RF}) \cdot Z_{BB}(f_{RF} - m \cdot f_{LO}). \tag{5.15}$$

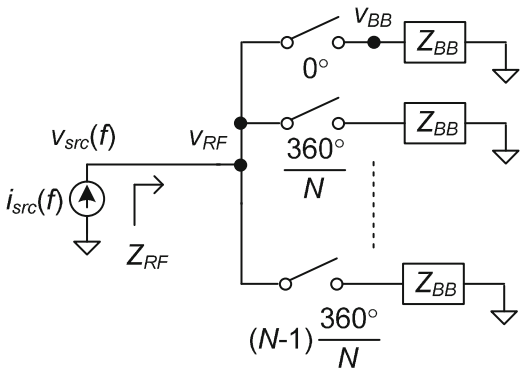

Fig. 5.22 A general N-phase switching system

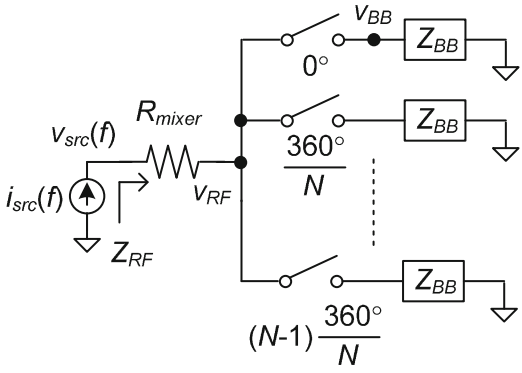

Fig. 5.23 General N-phase switching system modeling switch-on resistance (R_{mixer})

The factor N results from the fact that N contribution by N paths add up in phase at the RF side. As each path goes through down-and-up-conversion by the same LO signal, the total phase shift is zero (although the baseband signals *do* have different phases and different t_0 (5.14)). This adding can simultaneously occur for different frequency shifts, so that the total RF voltage is the sum of contributions from all LO-harmonics ($m = \ldots -1,\ 0,\ 1,\ \ldots$):

$$v_{RF}(f_{RF}) = i_{src}(f_{RF}) \cdot \sum_{m=-\infty}^{\infty} [N \cdot H(-m) \cdot H(m) \cdot Z_{BB}(f_{RF} - m \cdot f_{LO})]. \tag{5.16}$$

We can define an impedance Z_{RF} now and substitute (5.16):

$$Z_{RF}(f_{RF}) = \frac{v_{src}(f_{RF})}{i_{src}(f_{RF})} = \frac{v_{RF}(f_{RF})}{i_{src}(f_{RF})} = N \cdot \sum_{m=-\infty}^{\infty} [H(-m) \cdot H(m) \cdot Z_{BB}(f_{RF} - m \cdot f_{LO})] \tag{5.17}$$

Now let us include the finite switch-on resistance which can be modeled as a single R_{mixer} in front of the mixer, as shown in Fig. 5.23 (assuming equal paths and always exactly one current-path). Then we can write:

$$v_{src}(f_{RF}) = v_{RF}(f_{RF}) + i_{src}(f_{RF}) \cdot R_{mixer}. \tag{5.18}$$

And the impedance becomes:

$$Z_{RF}(f_{RF}) = \frac{v_{src}(f_{RF})}{i_{src}(f_{RF})} = R_{mixer} + N \cdot \sum_{m=-\infty}^{\infty} [H(-m) \cdot H(m) \cdot Z_{BB}(f_{RF} - m \cdot f_{LO})]. \tag{5.19}$$

In practice we want Z_{BB} to be a low-pass filter that strongly suppresses the high-frequency components. Equation (5.19) can then be simplified since only contributions of $Z_{BB}(f_{RF} - m \cdot f_{LO})$ at difference frequencies close to zero are significant. Defining an offset frequency Δf as $f_{RF} - m \cdot f_{LO}$, with $|\Delta f| \leq f_{LO}/2$, $(m \cdot f_{LO} + \Delta f) \geq 0$, and $m = 0,\ 1,\ 2,\ 3\ldots$, (5.19) can be rewritten as:

$$Z_{RF}(m \cdot f_{LO} + \Delta f) \approx R_{mixer} + N \cdot H(-m) \cdot H(m) \cdot Z_{BB}(\Delta f). \tag{5.20}$$

Substituting (5.14) into (5.20) we obtain (5.3) for m $\neq 0$.

In [30] simulations are reported showing good agreement between the previously derived equations and simulations.

B. Conversion Gain Derivation

Since the mixer clock has 1/8 duty cycle and the IF outputs use a multiphase combination for HR, the receiver conversion gain derivation is a bit more complex than for conventional receivers, and will be derived here. Using Fourier analysis, the magnitude (M) of the fundamental tone of a balanced 1/8 duty-cycle clock can be written as:

$$M = \frac{4}{\pi} \cdot \sin\frac{\pi}{8}. \tag{5.21}$$

For the first stage, there are three mixer outputs driven by three adjacent clock phases to be combined as one output (Fig. 5.6) with a weighting ratio of 2:3:2. Relative to the output with weight factor 3, the paths with weight 2 experience a phase of $+/-\pi/4$. The combined current flows through the feedback resistor (R_{f1}) of the 1st-stage TIA (TIA1). The gain from the differential input of LNTA to the differential output of TIA1 (Fig. 5.5) can be derived as:

$$\begin{aligned} G_1 &= \frac{M}{2} \cdot \left(2G_m \cdot \cos\left(+\frac{\pi}{4}\right) + 3G_m + 2G_m \cdot \cos\left(-\frac{\pi}{4}\right)\right) \cdot R_{f1} \\ &= \frac{M}{2} \cdot \left(3 + 4 \cdot \cos\frac{\pi}{4}\right) \cdot G_m \cdot R_{f1}. \end{aligned} \tag{5.22}$$

In (5.22), the multiplication factor is $M/2$, because in a mixing operation, only half of the signal is downconverted to baseband and the other half gets upconverted.

For the second stage, there are also three adjacent IF-signal phases from TIA1 combined as one output (Fig. 5.7) with a weighting ratio of 5:7:5 and a phase

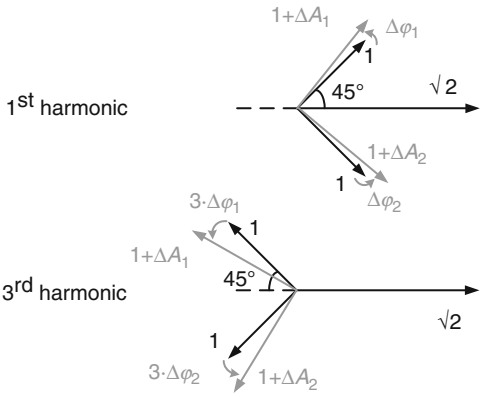

Fig. 5.24 Vector diagram modeling amplitude and phase errors for 8-phase harmonic rejection

differences of $+/-\pi/4$ for the paths with weight factor 5 compared to the path with weight 7. Assume for the 2nd-stage TIA (TIA2), the unit input resistor is R_{in2} and the feedback resistor is R_{f2}. The gain from the differential output of TIA1 to the differential output of TIA2 (Fig. 5.5) can be derived as:

$$\begin{aligned} G_2 &= \left(2\cdot\cos\frac{\pi}{8}\right)\cdot\frac{1}{R_{in2}}\left(\frac{1}{7}\cdot\cos\left(+\frac{\pi}{4}\right)+\frac{1}{5}+\frac{1}{7}\cdot\cos\left(-\frac{\pi}{4}\right)\right)\cdot R_{f2} \\ &= 2\cdot\cos\frac{\pi}{8}\cdot\left(\frac{1}{5}+\frac{2}{7}\cos\frac{\pi}{4}\right)\cdot\frac{R_{f2}}{R_{in2}}. \end{aligned} \tag{5.23}$$

In (5.23), the coefficient of $2\cdot\cos(\pi/8)$ comes from the fact that the 8-phase outputs of TIA1 are combined into the 4-phase outputs of TIA2 (Fig. 5.5). Equivalently, every two adjacent phases (with a difference of $\pi/4$) are combined into one, therefore the resulting vector has a phase difference of $+/-\pi/8$ from the two original vectors.

C. *Effect of Random Amplitude and Phase Errors to Harmonic Rejection*

This appendix derives the HR ratio and its sensitivity to amplitude and phase errors. These effects have been partly considered in [1] and [22], however, the statistical nature of mismatch and the effect of using a balanced RF or balanced LO were not been included. We will also consider the effect of LO duty cycle "d".

Suppose we have three signal paths to the output (as in Figs. 5.4–5.8) and the signals are represented by vectors as in Fig. 5.24. The resulted 1st and 3rd harmonics can be respectively written as:

$$\begin{aligned} H_1 &= R_{H1}\cdot\left[A_1\cos\varphi_1+\sqrt{2}\cos 0^\circ+A_2\cos\varphi_2\right] \\ H_3 &= R_{H3}\cdot\left[A_1\cos(3\varphi_1)+\sqrt{2}\cos 0^\circ+A_2\cos(3\varphi_2)\right], \end{aligned} \tag{5.24}$$

where R_{H1} and R_{H3} are the Fourier series coefficients of a pulse-wave LO with duty cycle "d":

$$\begin{aligned} R_{H1} &= \frac{2}{\pi}\sin(\pi\cdot d), R_{H3} = \frac{2}{3\pi}\sin(3\pi\cdot d), \\ A_1 &= (1+\Delta A_1), A_2 = (1+\Delta A_2), \\ \varphi_1 &= (45^\circ+\Delta\varphi_1), \varphi_2 = (-45^\circ+\Delta\varphi_2). \end{aligned} \tag{5.25}$$

If ΔA_1, ΔA_2, $\Delta\varphi_1$, $\Delta\varphi_2$ are small and uncorrelated, we can approximate the variance in H_3 as:

$$\begin{aligned} {\sigma_{H3}}^2 \approx {R_{H3}}^2 \cdot \Bigg[&\left(\frac{\partial H_3}{\partial A_1}\right)^2 \cdot {\sigma_{A1}}^2 + \left(\frac{\partial H_3}{\partial A_2}\right)^2 \cdot {\sigma_{A2}}^2 \\ &+ \left(\frac{\partial H_3}{\partial \varphi_1}\right)^2 \cdot {\sigma_{\varphi 1}}^2 + \left(\frac{\partial H_3}{\partial \varphi_2}\right)^2 \cdot {\sigma_{\varphi 2}}^2 \Bigg]. \end{aligned} \tag{5.26}$$

If $\sigma_{A1} = \sigma_{A2} = \sigma_A$ and $\sigma_{\varphi 1} = \sigma_{\varphi 2} = \sigma_\varphi$, then:

$${\sigma_{H3}}^2 \approx {R_{H3}}^2 \cdot \left[2\cos^2(3\cdot 45^\circ)\cdot {\sigma_A}^2 + 18\sin^2(3\cdot 45^\circ)\cdot {\sigma_\varphi}^2\right] = {R_{H3}}^2 \cdot \left[{\sigma_A}^2 + 9{\sigma_\varphi}^2\right]. \tag{5.27}$$

Since $H_1 \approx 2\sqrt{2}\cdot R_{H1}$, taking the ratio, we obtain:

$$\left(\frac{{\sigma_{H3}}^2}{{H_1}^2}\right) \approx \frac{{R_{H3}}^2 \cdot \left[{\sigma_A}^2 + 9{\sigma_\varphi}^2\right]}{8{R_{H1}}^2} = \frac{\sin^2(3\pi\cdot d)}{\sin^2(\pi\cdot d)} \left[\left(\frac{\sigma_A}{6\sqrt{2}}\right)^2 + \left(\frac{\sigma_\varphi}{2\sqrt{2}}\right)^2\right]. \tag{5.28}$$

Please note that σ_A is the standard deviation of amplitude error in percentage and σ_φ is the standard deviation of phase error in radians.

In a double-balanced HR mixer, which creates the output during one half period from 0 to $T/2$ with the positive-sign RF-LNTA path and the other half from $T/2$ to T with the negative-sign RF-LNTA path, the 1st harmonic adds up in amplitude while the 3rd harmonic adds up in power (as the error is uncorrelated between twohalf periods for both amplitude and phase). Therefore, the ratio is improved by 3 dB for a double-balanced HR mixer compared to (5.28), i.e.

$$\left(\frac{{\sigma_{H3}}^2}{{H_1}^2}\right)_{diff} \approx \frac{\sin^2(3\pi\cdot d)}{\sin^2(\pi\cdot d)} \left[\left(\frac{\sigma_A}{12}\right)^2 + \left(\frac{\sigma_\varphi}{4}\right)^2\right]. \tag{5.29}$$

If the duty cycle of the LO is 50% or 25%, i.e. $d = 0.5$ or 0.25, we get

$$\left({\sigma_{H3}}^2/{H_1}^2\right)_{diff,50\%} \approx \left(\sigma_A/12\right)^2 + \left(\sigma_\varphi/4\right)^2. \tag{5.30}$$

If there is no amplitude error, 50% or 25% duty cycle results in a 3σ-HR3 of 70 dB if $\sigma_\varphi = 0.024^\circ$.

If the duty cycle is 1/8, i.e. $d = 0.125$, as in our case, we get:

$$\left(\sigma_{H3}{}^2/H_1{}^2\right)_{diff,12.5\%} \approx 5.8 \cdot \left[\left(\sigma_A/12\right)^2 + \left(\sigma_\varphi/4\right)^2\right]. \tag{5.31}$$

Without amplitude error, the 3σ-HR3 is now 62 dB.

A similar derivation for 5th order HR of a double-balanced HR mixer renders:

$$\left(\frac{\sigma_{H5}{}^2}{H_1^2}\right)_{diff} \approx \frac{\sin^2(5\pi \cdot d)}{\sin^2(\pi \cdot d)} \cdot \left[\left(\frac{\sigma_A}{20}\right)^2 + \left(\frac{\sigma_\varphi}{4}\right)^2\right]. \tag{5.32}$$

where the phase term σ_φ would have been multiplied by 5 in (5.28) due to the 5-times phase shift of H_5 compared to H_1. Nevertheless, without amplitude errors, this leads to the same numerical result ($\sigma_\varphi = 0.024°$): a 3σ-HR5 of 62 dB for 1/8 duty cycle LO.

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Chapter 6
Reconfigurable Analog Baseband Filter

Masaki Kitsunezuka, Shinichi Hori, and Tadashi Maeda

6.1 Introduction

Demands for software defined radio (SDR) technologies enabling a device to handle both current and future wireless standards with changes only to software are increasing as next-generation wireless communication systems come closer to reality [1,2].

A key building block of SDR is the analog baseband (ABB) integrated circuit (IC), which consists of a baseband filter and a programmable gain amplifier (PGA) and has high reconfigurability to support a wide variety of standards. Figure 6.1 shows the spectra of desired and blocker signals for WCDMA and GSM, which are widely used standards for cellular phones. There are very large blockers close to the desired signal, and the baseband filter has to sufficiently attenuate them. It should be noted that each standard has a different channel bandwidth. This means that the baseband filter characteristics such as cut-off frequency, selectivity (filter order, pole/zero locations), and real or complex should be changed to meet the standard's specific requirements. Moreover, SDR requires scalability of power consumption so that it can meet the specifications of each standard with power consumption comparable to that of a single-mode radio.

Although conventional analog filters with a bias voltage control scheme are small in area and have low power consumption, their tuning range is limited especially with the low supply voltage used in advanced CMOS technologies. Filters configured in an array have a certain level of flexibility, but the die area is limited

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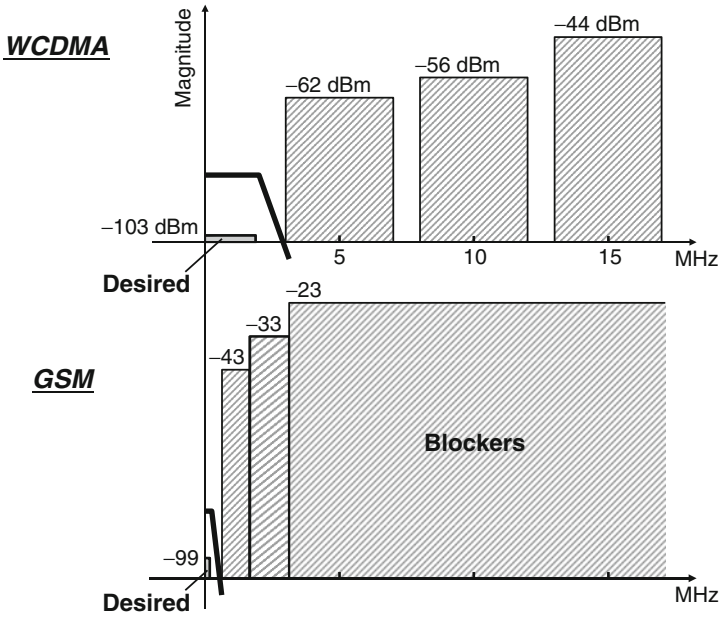

Fig. 6.1 Spectra of desired and blocker signals for WCDMA and GSM

by the device size to suppress flicker noise and/or to control device mismatch [2,3]. Although charge-domain discrete-time (DT) filtering techniques using passive switched capacitors have good flexibility, they cannot achieve high selectivity [9].

In this chapter, a new DT signal processing technique is introduced that solves these problems, and its application to the ABB IC is described. We developed a prototype ABB IC with wide-bandwidth tunability and filter transfer function reconfigurability. Section 6.2 describes the circuit's architecture and implementation, which includes a newly developed DT transconductor. Section 6.3 describes its measured performance, and Sect. 6.4 concludes this chapter with a brief summary of the key points and remarks about the applicability of the developed ABB IC.

6.2 Architecture and Circuit Design

6.2.1 Architecture

The direct-conversion receiver is well suited for SDR as it has the highest potential for reducing cost, size, and power. The developed ABB IC would be used as a building block of such a receiver, as shown in Fig. 6.2. The ABB IC, depicted in Fig. 6.3, comprises PGA1 for coarse gain tuning, followed by a passive low-pass filter (LPF) for anti-aliasing, two cascade-connected DT LPFs (DT LPF1,

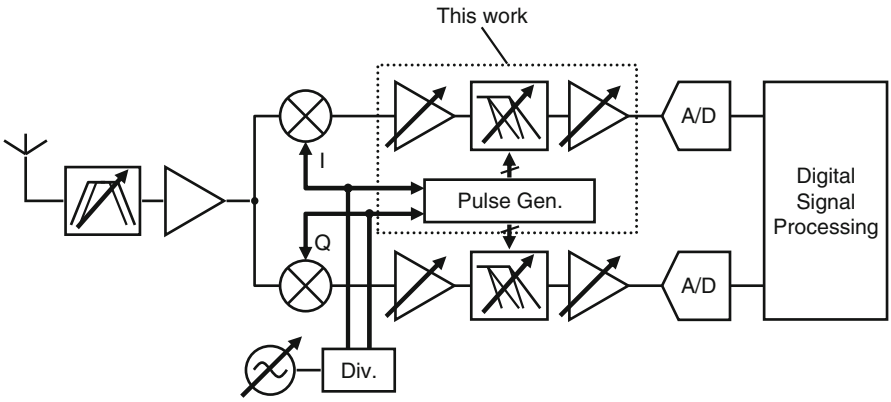

Fig. 6.2 Block diagram of SDR receiver

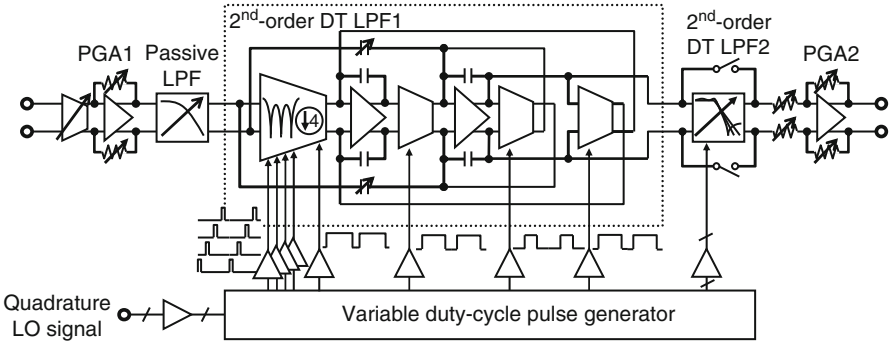

Fig. 6.3 Block diagram of developed analog baseband IC

DT LPF2) for channel selection, PGA2 for fine gain tuning, and a pulse generator for controlling the DT LPFs. All circuits in the baseband chain were designed to be fully differential to achieve a wide dynamic range; the differential configuration provides a large signal swing and cancellation of unwanted signals, such as even harmonics, common-mode noises, clock feed-through, and charge injection errors.

PGA1 consists of a conventional input transconductor array followed by an op-amp with a feedback resistor array. The use of a transconductor as the input stage means that the preceding mixer does not need to be able to handle resistive loads. The DT LPF designs are based on a second-order *Gm-C* filter with independently controlled transconductors; the filter characteristics can be tuned by simply changing the duty cycle of the control pulses. Two cascade-connected second-order DT LPFs provides fourth-order filtering. One of the main advantages of cascade filter configurations is that they are very easy to adjust because each second-order cell is responsible for the realization of only one pole pair and zero pair [8]. To achieve effective anti-aliasing, the input transconductor, which is the first stage

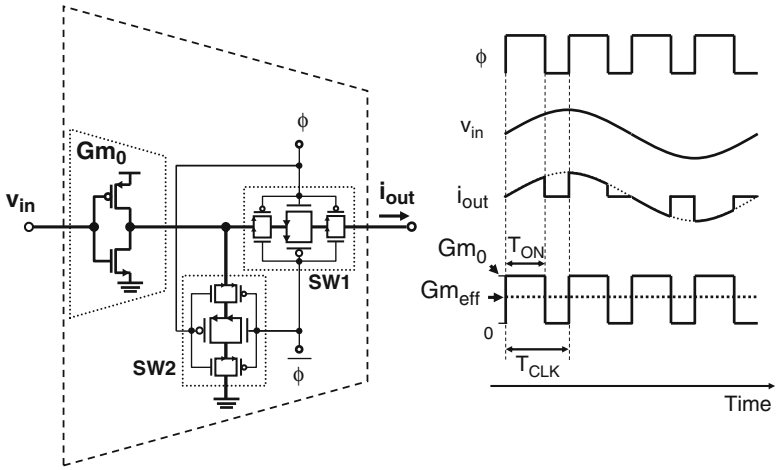

Fig. 6.4 Duty-cycle-controlled discrete-time transconductor

of the DT LPF1, was designed to perform four-tap finite-impulse-response (FIR) filtering during voltage-to-current conversion. A second-order filter response can be obtained by bypassing the second second-order cell (DT LPF2). PGA2 has a circuit similar to that of PGA1, but it uses a resistor array as the input stage. Since the gain is determined by the ratio of the feedback resistance value to the input one, this configuration has a high tolerance for process, voltage, and temperature (PVT) variations.

Quadrature local oscillator (LO) signals are used as inputs to the pulse generator even though the LO frequency is different for each wireless standard. This is because the filter characteristics depend on the duty cycle of the control pulses, not the clock frequency. Essentially, the DT LPF needs only a control pulse with a frequency higher than twice the signal bandwidth. If needed, other approaches can be used to generate various duty-cycle pulses, such as using a self-oscillation circuit.

6.2.2 Duty-Cycle-Controlled Discrete-Time Transconductor

The concept of the proposed duty-cycle controlled DT transconductor is shown in Fig. 6.4. A single-ended version is depicted for simplicity. The transconductor consists of a core and two switches. A CMOS-inverter-based transconductor is used as the core in this implementation because of its high-frequency performance and high linearity [7]. The switches are CMOS transmission gates with half-sized dummies to cancel the clock feed-through and charge injection errors.

The switchings of SW1 and SW2 are controlled by clock pulse ϕ and its inverse $\overline{\phi}$, respectively. The clock period of ϕ is T_{CLK}, and the duration of high-level is T_{ON}. Example waveforms of an input voltage (v_{in}) and an output current (i_{out}) are also shown in Fig. 6.4. When ϕ is high and SW1 is in the ON state, the output current

of the transconductor core is fed into the following stage. When ϕ is low and SW1 is in the OFF state, SW2 turns on and the output current of the transconductor core flows to the ground. SW2 prevents the output current of the core from being fed into parasitic capacitors and causing an error when SW1 is in the ON state.

To discuss the time-averaged transconductance gain, we define clock pulse ϕ as

$$\phi(t) = \begin{cases} 1, & 0 \le t \le T_{\mathrm{ON}} \\ 0, & \text{otherwise.} \end{cases} \tag{6.1}$$

The gain of this transconductor is time-variant: it is Gm_0 when ϕ is high and zero otherwise, where Gm_0 is the transconductance gain of the core. The signal charge transferred to the following stage during the nth sampling period can be expressed as

$$\begin{aligned} Q_{\mathrm{sig}} &= \int_{nT_{\mathrm{CLK}}}^{(n+1)T_{\mathrm{CLK}}} Gm_0 v_{\mathrm{in}}(\tau) \cdot \phi(nT_{\mathrm{CLK}} + T_{\mathrm{ON}} - \tau)\,\mathrm{d}\tau \\ &= \frac{\mathrm{e}^{j\omega T_{\mathrm{ON}}} - 1}{j\omega} \mathrm{e}^{j\omega(nT_{\mathrm{CLK}} - t)} Gm_0 v_{\mathrm{in}}(t), \end{aligned} \tag{6.2}$$

where $v_{\mathrm{in}}(t)$, a hypothetical complex sinusoid of frequency ω, is the input voltage signal. Since a time-averaged signal current is given by $\overline{i_{\mathrm{sig}}} = Q_{\mathrm{sig}}/T_{\mathrm{CLK}}$, the time-averaged effective transconductance gain is given by

$$Gm_{\mathrm{eff}} = \frac{\overline{i_{\mathrm{sig}}}}{v_{\mathrm{in}}} = \frac{\mathrm{e}^{j\omega T_{\mathrm{ON}}} - 1}{j\omega T_{\mathrm{CLK}}} \mathrm{e}^{j\omega(nT_{\mathrm{CLK}} - t)} Gm_0. \tag{6.3}$$

Under the condition that the input frequency is low compared with the clock frequency, (6.3) can be approximated as

$$Gm_{\mathrm{eff}} \sim \frac{T_{\mathrm{ON}}}{T_{\mathrm{CLK}}} Gm_0. \tag{6.4}$$

Equation (6.4) means that Gm_{eff} can be controlled by setting the ratio of T_{ON} to T_{CLK}, which is the duty-cycle of the clock pulse.

Since the DT transconductor operates like a switching mixer, noise folding occurs: wideband noises, such as thermal noise, are down-converted to the baseband frequency. In contrast, flicker noise, which contributes at low frequencies, does not experience noise folding. In any case, the flicker noise level is minimized due to the use of a large transconductor core and low duty-cycle control pulses even though a small transconductance gain is required for a narrowband filter. Thus, only thermal noise is analyzed here. Provided that the input-referred thermal noise voltage of the transconductor core in the frequency range Δf is expressed as

$$\overline{v_{\mathrm{th}}^2} = \frac{4kT\gamma}{Gm_0} \Delta f, \tag{6.5}$$

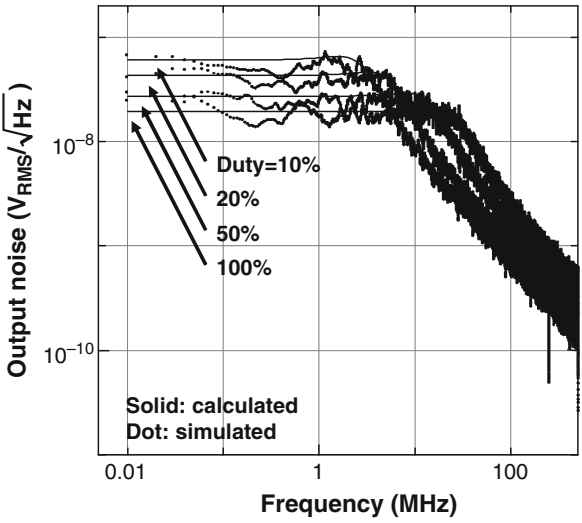

Fig. 6.5 Output noise spectrum of DT-transconductor-based filter for various duty cycles

where γ is the thermal noise coefficient, the output noise current is given by

$$\overline{i_{\text{th}}^2} = |Gm_{\text{eff}}|^2 \overline{v_{\text{th}}^2}. = \left(\frac{T_{\text{ON}}}{T_{\text{CLK}}} Gm_0\right)^2 \text{sinc}^2\left(\frac{\omega T_{\text{ON}}}{2}\right) \overline{v_{\text{th}}^2}, \tag{6.6}$$

where $\text{sinc}(x)$ denotes the function $\sin(x)/x$. If the noises above $f_{\text{CLK}}/2$ are considered to be folded into the Nyquist band ($0 < f < f_{\text{CLK}}/2$), the output noise current can be calculated as

$$\begin{aligned}\overline{i_{\text{n,out}}^2} &= \int_0^\infty \overline{i_{\text{th}}^2} \text{d}f \Big/ \frac{f_{\text{CLK}}}{2} \\ &= 8kT\gamma \frac{T_{\text{ON}}}{\pi T_{\text{CLK}}} Gm_0 \Delta f \int_0^\infty \text{sinc}^2\left(\frac{\omega T_{\text{ON}}}{2}\right) \text{d}\left(\frac{\omega T_{\text{ON}}}{2}\right).\end{aligned} \tag{6.7}$$

Since the integral in (6.7) gives $\pi/2$, we get

$$\overline{i_{\text{n,out}}^2} = 4kT\gamma \left(\frac{T_{\text{ON}}}{T_{\text{CLK}}} Gm_0\right) \Delta f, \tag{6.8}$$

which means that the output noise current of the duty-cycle-controlled DT transconductor is equal to that of an equivalent continuous-time (CT) transconductor with a transconductance gain of $(T_{\text{ON}}/T_{\text{CLK}})\,Gm_0$. Another approach using a harmonic transfer function in a linear periodically time-varying system also leads to the same results [6]. Figure 6.5 shows simulated output noise spectra for a DT-transconductor-based low-pass filter for duty cycles from 10% to 100%. The effect of flicker noise was neglected in the simulation. The value calculated using (6.8) agrees well with the result of transient analysis.

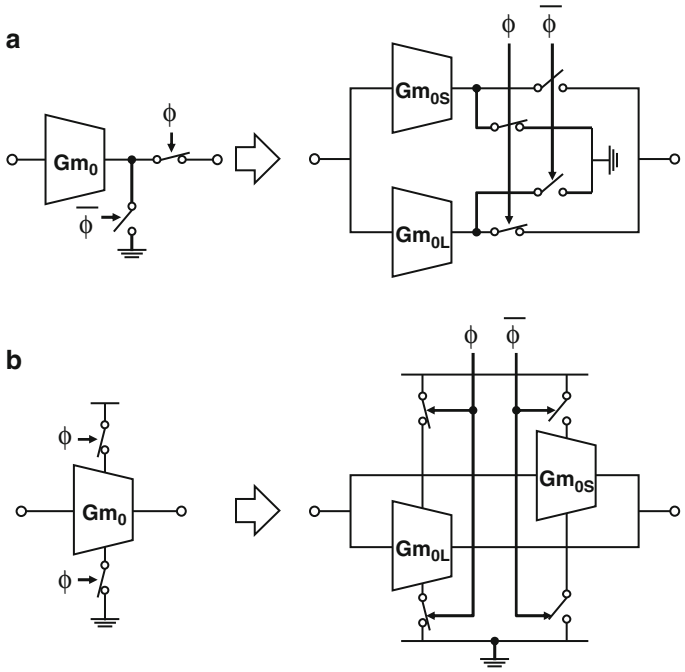

Fig. 6.6 Other configurations of duty-cycle-controlled discrete-time transconductor: **(a)** switches connected to transconductor core output nodes and **(b)** switches connected to voltage supply and ground nodes

While the discussion so far has focused on simple on/off switching of a single transconductor core, the complementary switching of two cores with different transconductance gains is also possible, as shown in Fig. 6.6a. When two transconductance gains given by Gm_{0L} and Gm_{0S} ($Gm_{0L} > Gm_{0S}$) are time-averaged, the effective transconductance gain is expressed as

$$Gm_c = \left(\frac{T_{\mathrm{ON}}}{T_{\mathrm{CLK}}}\right) Gm_{0L} + \left(1 - \frac{T_{\mathrm{ON}}}{T_{\mathrm{CLK}}}\right) Gm_{0S}. \tag{6.9}$$

This complementary switching configuration relaxes the requirements for the anti-aliasing filter (AAF) in comparison with a simple on/off switching one in exchange for a narrower tuning range of Gm_{0S} to Gm_{0L} [5]. In the prototype implementation, the simple on/off configuration was used in order to demonstrate wide tunability.

Another example implementation of the DT transconductor is depicted in Fig. 6.6b: a simple on/off switching configuration and complementary switching one. MOS switches connected to the voltage supply or ground result in low on-resistances even with small gates. This is because sufficiently high gate-source voltages are applied to the MOS switches even at a low supply voltage. This can reduce current consumption depending on the duty cycle, but the circuit wake-up time would limit the highest sampling frequency.

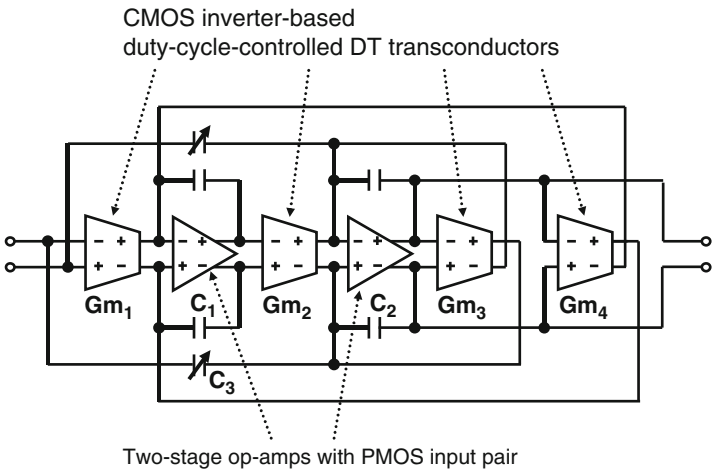

Fig. 6.7 Duty-cycle-controlled discrete-time low-pass filter

6.2.3 Reconfigurable DT Filter

A schematic of a second-order duty-cycle-controlled DT LPF is depicted in Fig. 6.7. This filter consists of DT transconductors, metal-insulator-metal (MIM) capacitors, and op-amps in a differential configuration to improve linearity performance at a low voltage supply (1.0 V). The advantage of using op-amps is that the output nodes of the transconductors are maintained at a specific operating point, so the circuits do not have to swing over a large voltage range. The virtual ground eliminates the non-ideal effects of the practical CMOS switches, such as non-linearity. That is, there is no charge/discharge of the parasitic capacitance, and the on-resistance is constant regardless the signal amplitude. Furthermore, since each transconductor drives an op-amp virtual ground, the time variation of the transconductor's output impedance due to the switching operation can be neglected.

The noise contribution from the op-amps in the DT LPF are the same as in the CT filter because the bandwidth of the op-amps is lower than the sampling frequency; the DT LPFs have only to suppress the blockers near the signal channel since the blockers over the Nyquist band have already been sufficiently removed by the AAF discussed later. A high-speed op-amp is not required for the same reason. As a result, some of the difficulties in circuit power and area are reduced. Fully differential two-stage op-amps with a PMOS input pair and push-pull output stages were used in this implementation to enable low flicker noise operation.

The transfer-function of this filter $H(s)$ is expressed as

$$H(s) = -\frac{\frac{C_3}{C_2}s^2 + \frac{Gm_1 Gm_2}{C_1 C_2}}{s^2 + \frac{Gm_3}{C_1}s + \frac{Gm_2 Gm_4}{C_1 C_2}}. \tag{6.10}$$

Equation (6.10) indicates that many kinds of filter responses can be obtained by simply changing each transconductance gain, Gm_i ($i = 1$–4). For example, cut-off frequency ω_c, zero frequency ω_z, and quality factor Q are given by

$$\omega_c = \sqrt{\frac{Gm_2 Gm_4}{C_1 C_2}} \tag{6.11}$$

$$\omega_z = \sqrt{\frac{Gm_1 Gm_2}{C_1 C_3}} \tag{6.12}$$

$$Q = \frac{\sqrt{Gm_2 Gm_4}}{Gm_3} \sqrt{\frac{C_1}{C_2}}, \tag{6.13}$$

so ω_c, ω_z, and Q can be tuned by adjusting Gm_2, C_3, and Gm_3, respectively. A capacitor array was used for C_3 to achieve an elliptic filter response.

Since the proposed tuning scheme needs only duty-cycle control, a wide tuning range is obtained even with a low supply voltage. Moreover, various duty-cycle pulses for the independent control of each DT transconductor can be generated with a digital logic circuit in a small area with low power consumption by using advanced CMOS technologies. These features enable multiple filter functions with few drawbacks.

Another advantage of the DT LPFs is that all DT transconductors can be designed for the same MOS size and bias voltage. This design approach results in high tolerance for PVT fluctuations, assuming that time-constant C/Gm is appropriately tuned. Although the tuning circuit was not implemented in the fabricated IC, many conventional tuning methods can be applied to the DT LPFs, for example, a switched-capacitor circuit or a phase-locked loop. Once time-constant C/Gm_0 is measured using one of these methods, the DT LPFs can compensate for variations in the duty cycle. Moreover, as described in 6.2.2, a large MOS device can be used in a narrowband filter as well as in a wideband one. This results in low-flicker noise characteristics. It should be noted, however, that (6.8) indicates that the lower limit of the cut-off frequency of the DT LPFs is determined by the following analog-to-digital converter dynamic range requirement for practical use.

6.2.4 Anti-aliasing Filter

In the duty-cycle-controlled DT LPFs, the blockers around the multiples of the clock frequency should be eliminated beforehand so as not to be down-converted to the passband of the DT LPFs, like other discrete-time filters such as the switched-capacitor filter. In terms of minimizing the effects on power and area, an anti-aliasing function was implemented by using a passive LPF with resistor and capacitor arrays and a voltage-input current-output four-tap FIR filter combined with the duty-cycle control scheme, as shown in Fig. 6.8. The four-tap FIR filter is merged into the first stage of the DT LPF and it does not need large passive components.

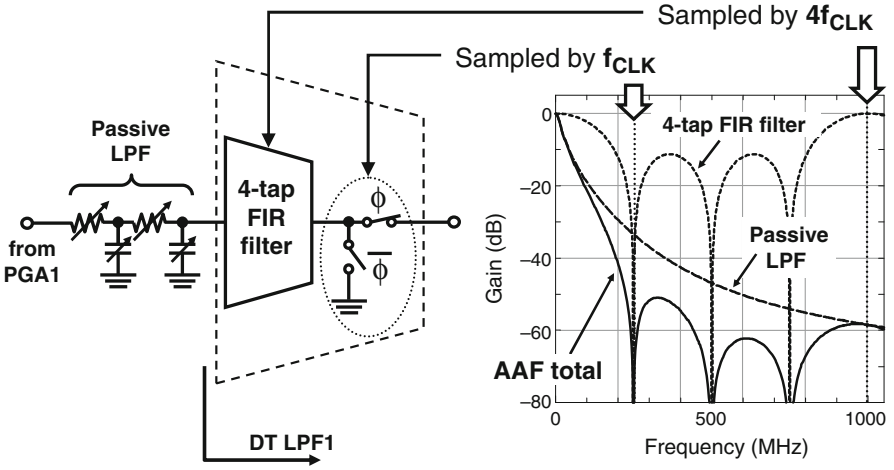

Fig. 6.8 Anti-aliasing filter (passive LPF + four-tap FIR filter)

The component values of the passive LPF are set so that it can attenuate high-frequency blockers and noises greater than four times the f_{CLK}, which is the sampling frequency of the four-tap FIR filter. The effect of a PVT variation is not problematic because the passive LPF does not need steep cut-off characteristics, and its cut-off frequency is much higher than that of the DT LPFs.

The following four-tap FIR filter effectively suppresses the noises down-converted to the passband of the DT LPF because it has notches at f_{CLK}, $2f_{CLK}$, and $3f_{CLK}$, as shown by the frequency characteristics in Fig. 6.8. The FIR filter does not need a tuning circuit because the notch frequencies depend only on the sampling frequency.

As shown in Fig. 6.9, the four-tap FIR filter comprises four transconductor cores and four input sampling switches. The input sampling switches are driven by four-phase time-interleaved clock pulses. The input signal voltage is alternately sampled and held on each parasitic gate capacitor, and each transconductor core outputs the corresponding current. The output currents of each transconductor core when ϕ_1 is high are drawn on the figure as an example. Four-tap FIR filtering is achieved by summing the output currents of each transconductor core in the current domain.

The transconductance gain is expressed by

$$Gm_{\mathrm{FIR4}}(z) = \frac{1 + z^{-1} + z^{-2} + z^{-3}}{4} Gm_{\mathrm{eff}}, \tag{6.14}$$

where z^{-1} is $\exp(-j\omega T_{CLK}/4)$, and it denotes a delay of one sampling period ($T_{CLK}/4$). Equation (6.14) shows that this circuit provides a moving average filter transfer function multiplied by Gm_{eff}. Achieving sufficient attenuation at the notches requires that the on-times of the four-phase pulses, T_S, be short compared with the hold-time, $T_H = T_{CLK}/4 - T_S$.

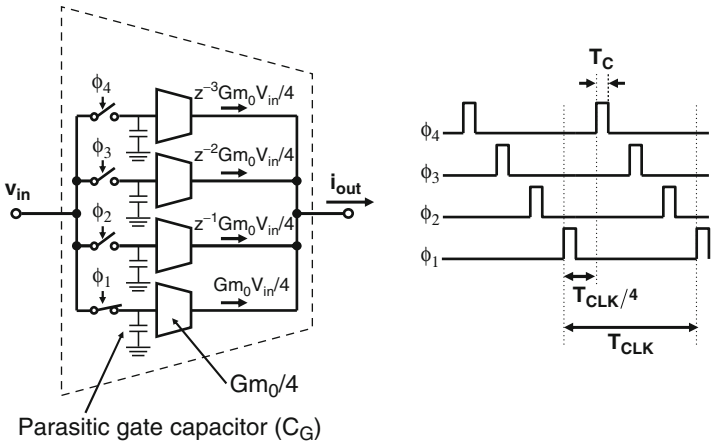

Fig. 6.9 Voltage-input current-output four-tap FIR filter

The effect of noise folding on voltage sampling in the filter's input stage, which has been well studied for conventional switched-capacitor filters [4], must be considered. The noises of a voltage sampling circuit can be divided into direct noises caused by each transconductor core during a high-level clock period and sampled-and-held (S/H) noises during a low-level period. Since direct noise contributes only during a short time compared to the hold time, it can be neglected. S/H noise in the Nyquist band ($0 < f < 2f_{\mathrm{CLK}}$) is estimated using

$$\begin{aligned}\overline{v_{n,\mathrm{S/H}}^2} &= \left(\frac{T_\mathrm{H}}{T_\mathrm{S}+T_\mathrm{H}}\right)^2 \mathrm{sinc}^2\left(\frac{\omega T_\mathrm{H}}{2}\right)\cdot\int_0^\infty \frac{4kTR_\mathrm{ON}}{1+\omega^2R_\mathrm{ON}^2C_\mathrm{G}^2}\mathrm{d}f\times\Delta f\Big/2f_\mathrm{CLK}\\ &= \left(\frac{T_\mathrm{H}}{T_\mathrm{S}+T_\mathrm{H}}\right)^2 \mathrm{sinc}^2\left(\frac{\omega T_\mathrm{H}}{2}\right)\cdot\frac{kT\Delta f}{\pi f_\mathrm{CLK}C_\mathrm{G}}\int_0^\infty \frac{\mathrm{d}(\omega R_\mathrm{ON}C_\mathrm{G})}{1+(\omega R_\mathrm{ON}C_\mathrm{G})^2},\end{aligned}\tag{6.15}$$

where R_{ON} and C_{G} are the on-resistance of the switch and the gate capacitance, respectively. Since the sinc function is unity at low frequencies and the integral in (6.15) gives $\pi/2$, (6.15) can be written as

$$\overline{v_{n,\mathrm{S/H}}^2} \sim \left(\frac{T_\mathrm{H}}{T_\mathrm{S}+T_\mathrm{H}}\right)^2 \frac{kT}{2f_\mathrm{CLK}C_\mathrm{G}}\Delta f.\tag{6.16}$$

With current-mode four-tap FIR filtering, the S/H noises around the multiples of f_{CLK} can be attenuated as

$$\overline{i_{n,\mathrm{S/H}}^2} = |Gm_{\mathrm{FIR4}}|^2\,\overline{v_{n,\mathrm{S/H}}^2}.\tag{6.17}$$

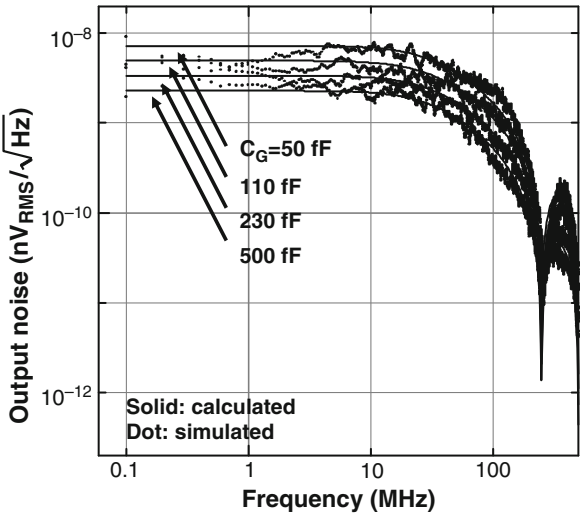

Fig. 6.10 Output noise spectra of four-tap FIR filter for various gate capacitances C_G

However, the passband noises cannot be suppressed. Thus, in our design, we maximized $f_{CLK}C_G$ so that the passband noise contribution by (6.17) is small compared with the folding thermal noise of DT transconductors given by (6.8). Figure 6.10 shows the simulated output noise spectra of the four-tap FIR filter for various input capacitances. The output noise current was converted into voltage by a noiseless resistor in this simulation. This result does not include the effect of flicker noise. The noise level calculated using (6.17) closely matches the results of transient analysis.

Another design issue with this circuit is linearity degradation. If sampling time T_S is not long enough to charge the input voltage signal on the parasitic gate capacitors, there will be a gain loss. If on-resistance R_{ON} is assumed to be linear, the voltage across the gate capacitor C_G for sampling time T_S can be expressed as

$$v_{C_G} = v_{in}\left(1 - e^{-\frac{T_S}{R_{ON}C_G}}\right). \tag{6.18}$$

The relative error caused by the insufficient sampling time is given by

$$\varepsilon = \frac{v_{in} - v_{C_G}}{v_{in}} = e^{-\frac{T_S}{R_{ON}C_G}}. \tag{6.19}$$

We set T_S and $R_{ON}C_G$ so that ε was about 0.1%.

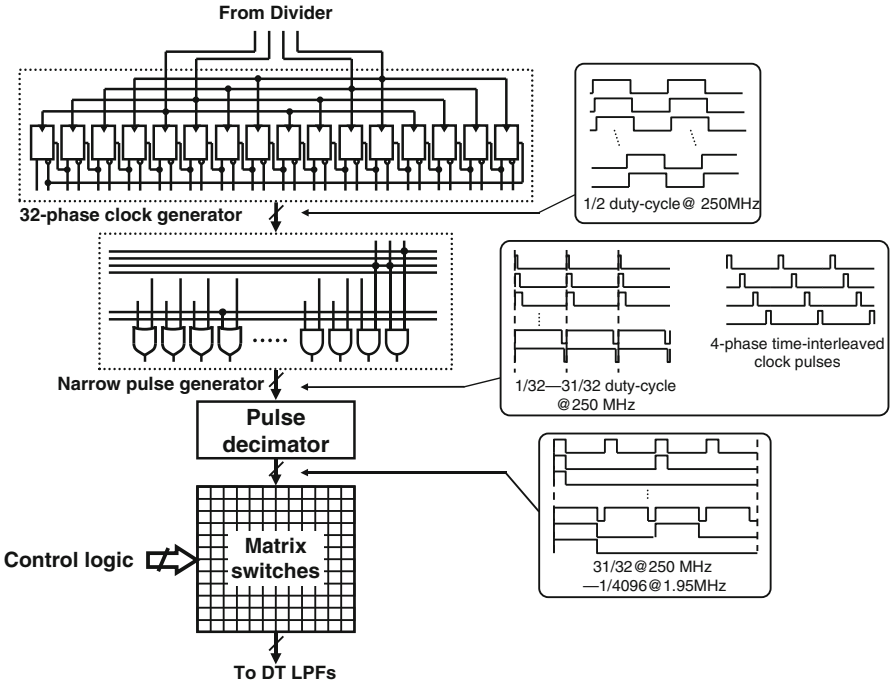

Fig. 6.11 Variable duty-cycle pulse generator

6.2.5 Variable Duty-Cycle Pulse Generator

As shown in Fig. 6.11, the variable duty-cycle pulse generator consists of a 32-phase clock generator, a narrow pulse generator, a pulse decimator, and matrix switches. This generator can provide a wide range of duty-cycle pulses to the DT LPFs through a simple change in the control logic data stream using a serial-to-peripheral interface.

The clock generator has a circuit similar to that of a shift counter with D-type flip-flops (DFFs), and it uses 2-GHz four-phase clocks as inputs. Each DFF is driven by a clock shifted 90° from the previous clock, and its data output terminal is connected to the data input terminal of the following DFF. As a result of the counting process, the input clocks are divided by 16, so 32-phase clocks with a 50% duty cycle at 250 MHz are obtained. The narrow pulse generator provides various duty-cycle pulses from 1/32 to 31/32 by performing the AND/OR operation of the 32-phase clocks. The four-phase time-interleaved clock pulses for the four-tap FIR filter can also be generated by changing the input signal combination.

When a very narrowband filter is required, the pulse decimator generates very low duty-cycle pulses (down to 1/4096) by decimating the pulses. The decimation is done using an AND operation with a narrow pulse and a divided clock of the narrow

pulse itself. The following matrix switches select the desired duty-cycle pulses in accordance with the control logic, and the selected pulses are buffered and provided to the DT LPFs.

Here, we focus on the contribution of clock jitter to the noise performance of the DT LPFs. Because Gm_{eff} is proportional to T_{ON}, clock jitter induces a fluctuation of Gm_{eff} and leads to noise. If the standard deviation of the sampling clock is given by δt, the error charge can be expressed as $Q_{\mathrm{err}} = Gm_0 v_{\mathrm{in}} \delta t$. Therefore, from (6.2), the signal-to-noise ratio during one clock period can be written as

$$S/N = \frac{|Q_{\mathrm{sig}}|^2}{2|Q_{\mathrm{err}}|^2} \sim \frac{T_{\mathrm{ON}}^2}{2\delta t^2}. \tag{6.20}$$

However, the Q_{err} values are randomly distributed, so they can be canceled by integrating them over a long period. As a result, the jitter effect is much smaller than the thermal noise effect.

6.3 Measurement Results

The developed ABB IC, fabricated in 90-nm CMOS, has a core area of 0.57 mm^2. A die photograph of the prototype chip is shown in Fig. 6.12.

Figure 6.13 shows the measured frequency characteristics of a fourth-order Butterworth filter. The cut-off frequency could be tuned from 400 kHz to 30 MHz by changing the duty cycle of the control pulses. Figures 6.14a and 6.14b respectively

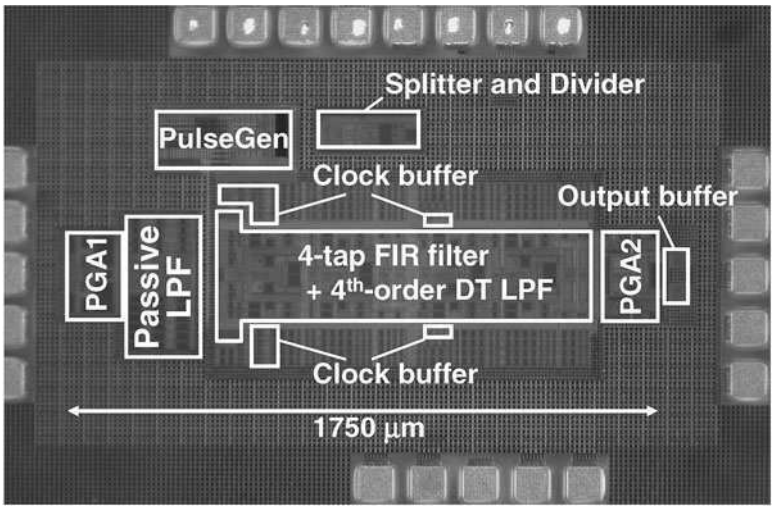

Fig. 6.12 Die photograph

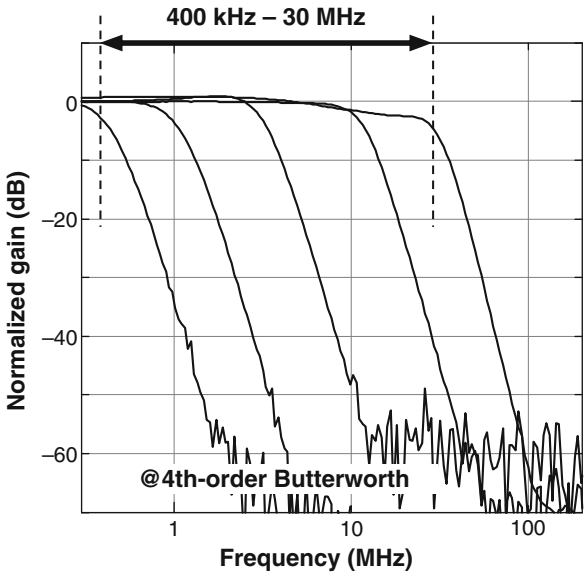

Fig. 6.13 Cut-off frequency tunability of fourth-order LPF

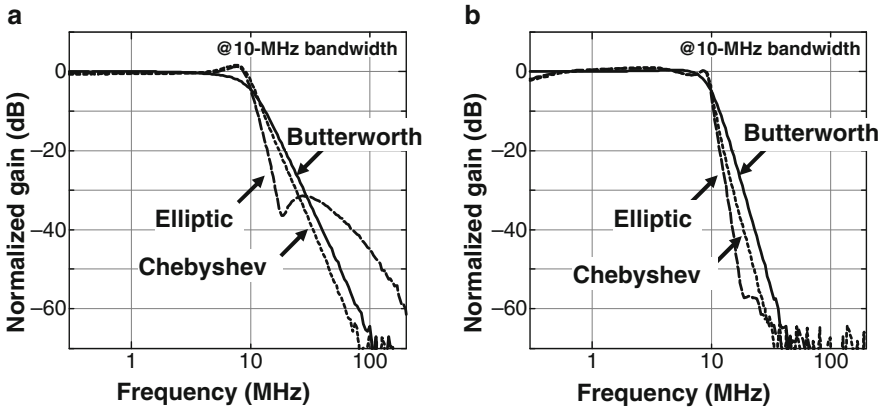

Fig. 6.14 Filter-type reconfigurability of (**a**) second- and (**b**) fourth-order LPFs

show the measured frequency characteristics of the second- and fourth-order filters in 10-MHz-bandwidth WLAN mode. The chip provided typical filters of Butterworth, Chebyshev, and elliptic responses.

Figures 6.15a,b illustrate the gain-tuning performance achieved by changing the gains of PGA1 and PGA2, respectively. PGA1 provided a gain range of -12 to $+24$ dB, with 12-dB steps (coarse tuning). PGA2 provided a gain range of 0 to 12 dB, with 0.5-dB steps (fine tuning).

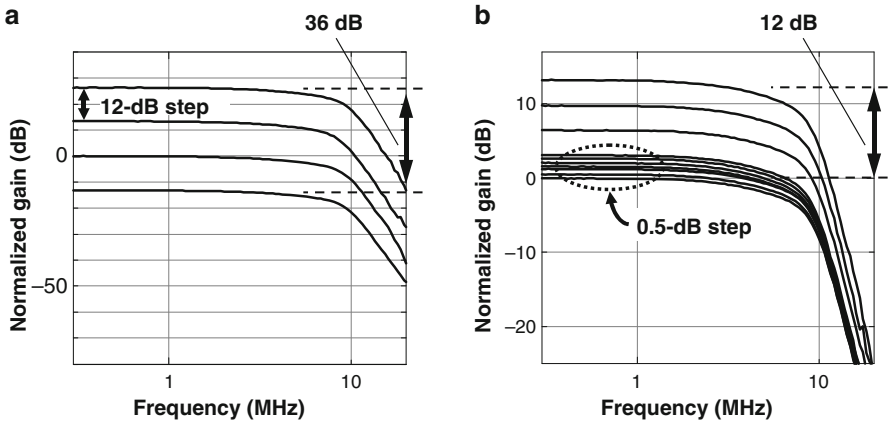

Fig. 6.15 (**a**) Coarse and (**b**) fine gain tunability

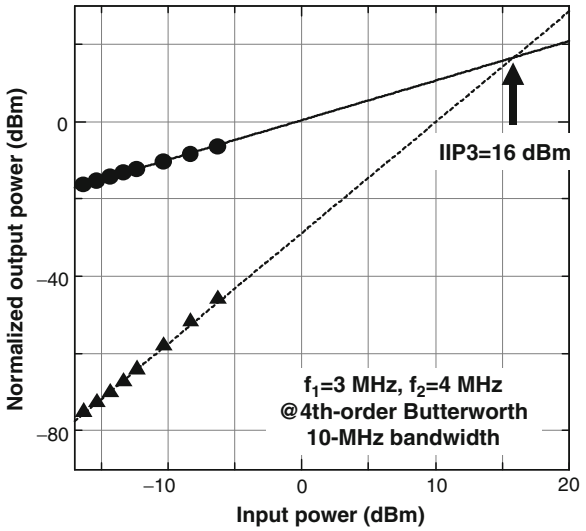

Fig. 6.16 Third-order input intercept point

The third-order input intercept point (IIP3) is shown in Fig. 6.16. Input two-tone signal frequencies were 3 and 4 MHz, and the voltage gains of the PGAs were set to zero. The filter was operated in fourth-order Butterworth WLAN mode. An IIP3 of +16 dBm was obtained with a 1.0-V supply. Figure 6.17 plots the 1-dB gain compression point. An input one-tone signal frequency was 3 MHz, and the filter operation mode was the same as before. The P1dB was +7 dBm with a 1.0-V supply.

Figure 6.18 shows the measured output noise spectrum. The dotted line represents a simulated fourth-order DT LPF using the analytical noise model described in Sect. 6.2; flicker noise was not considered. The measured noise floor in the passband

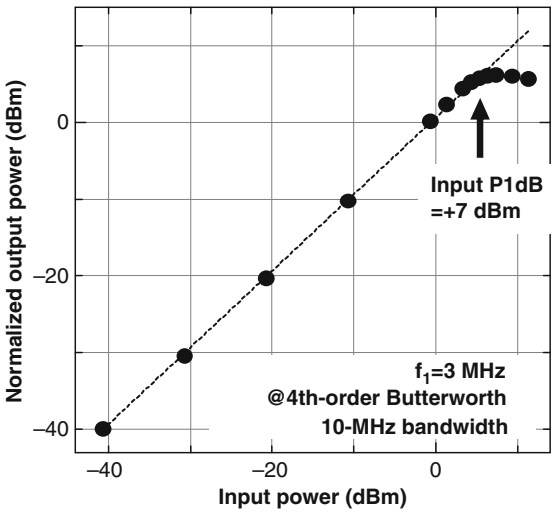

Fig. 6.17 1-dB gain compression point

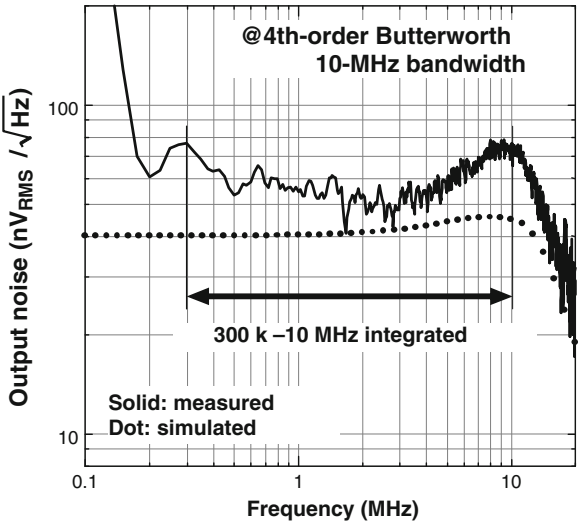

Fig. 6.18 Measured output noise spectrum

matches the simulated level. The input-referred noise was 98 $nV_{RMS}/\sqrt{Hz}$ under the condition that the voltage gains of the PGAs were zero. The input-referred integrated noise was 0.31 mV_{RMS}, with an integration range of 300 kHz to 10 MHz.

Table 6.1 summarizes the measured ABB IC performance values. The current consumption of the filter core was 5 mA, and that of the circuit in total was 12 mA with a 1.0-V supply, not including the current consumption of the clock divider followed by the pulse generator.

Table 6.1 Performance summary

Technology	90 nm-CMOS
Supply voltage	1.0 V
Filter order	2nd, 4th
Filter type	Butterworth, Chebyshev, Elliptic
Cut-off frequency range	400 kHz–30 MHz
IIP3 ($f_1 = 3$ MHz, $f_2 = 4$ MHz)	16 dBm
Input P1dB @3 MHz	7 dBm
Input-referred noise	0.31 mV_{RMS}
Gain range	55 dB
Gain step	0.5 dB
Current consumption	
DT LPFs	5 mA
PGAs	7 mA
Pulse gen.	1 mA
Core area	0.57 mm^2

6.4 Conclusion

The duty-cycle-controlled discrete-time filter introduced in this chapter enables the fabrication of an analog baseband circuit with wide-bandwidth tunability and filter transfer function reconfigurability. The key technical features of the developed circuit are a duty-cycle-controlled DT transconductor, a four-tap FIR filter for anti-aliasing, and a variable duty-cycle pulse generator. The measured performance of the test chip fabricated in 90-nm CMOS demonstrated the circuit's wide bandwidth tunability and the filter type/order reconfigurability.

Although only a low-pass filter configuration was described, the concept of the duty-cycle-controlled DT transconductor can easily be expanded to cover a complex band-pass filter for image rejection in order to support a low-intermediate-frequency receiver architecture. Since the developed ABB circuit has highly reconfigurable characteristics and is compact, it is well suited as a building block for software-defined radio transceivers.

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Chapter 7
Multi-Standard Data Converters

Akira Matsuzawa

7.1 Introduction

Analog-to-Digital converters (ADC) and Digital-to-Analog converters (DAC) are required in receivers and in transmitters, respectively. The required bandwidth of DAC is determined by communication standards and required resolution is dependent on modulation scheme, like quadrature phase shift keying (QPSK) or quadrature amplitude modulation (QAM), etc. Since current-mode DAC can deal with most of communication standards and modulation schemes, it is readily applied for multi-standard radios. On the other hand, compared to DACs, the situation of ADC is more complicated, because there are more factors that affect the required performance of ADC, such as the unwanted signal, performance of pre-filter, ratio of thermal noise and quantization noise, demodulation method and so on. In this chapter, we will mainly study ADC for multi-standard radios.

7.2 Wireless Communication Standards and Required Analog-to-Digital Converter Performance

In this section, we will describe various wireless communication standards and the required ADC performance.

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Table 7.1 Wireless communication standards and signal bandwidth f_b

Standard	f_b (MHz)
EDGE	0.1
GSM	0.2
CDMA	0.6
Bluetooth	1.0
WCDMA	1.9
DVB-H	4.0
LTE	5.0
WLAN 802.11a	10.0
WLAN 802.11n	20.0

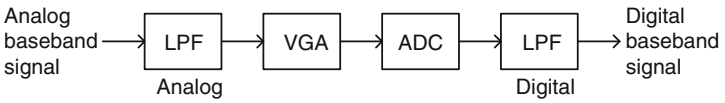

Fig. 7.1 Analog front-end of receivers

7.2.1 Signal Bandwidth

Table 7.1 shows the bandwidth f_b of typical wireless communication standards. The often used wireless communication standards are from EDGE with a bandwidth of 135 kHz to WLAN with a bandwidth of 20 MHz listed in Table 7.1.

7.2.2 Sampling Frequency

The required sampling frequency is theoretically at least more than twice as high as the signal bandwidth. However, considering the adjacent channel and unwanted signals, in fact, the sampling frequency should be even higher than that.

Figure 7.1 shows the analog front-end of receivers. As can be seen, a low-pass filter (LPF) and variable gain amplifier (VGA) are located before the ADC, which will affect the required performance of the ADC.

The required characteristics of the analog filter are shown in Fig. 7.2. For anti-aliasing filters, the magnitude of signals satisfying $f_s - f_b < f < f_s + f_b$, should be lower than the specified stop-band transmission value, A_{sb}, where, f_b is the baseband signal frequency and f_s is the sampling frequency of folded ADC converter.

A Butterworth filter is often used in a communication system as a basic filter since its frequency response is maximally flat and has no ripples in the passband. Let's study the frequency characteristics based on Butterworth filter. For an Nth-order Butterworth filter with maximum passband transmission, A_p, the frequency response in the range higher than the passband frequency, f_b, can be approximated as

$$A_{dB}(f) \approx -20N_p \log\left(\frac{f}{f_b}\right) - A_p. \tag{7.1}$$

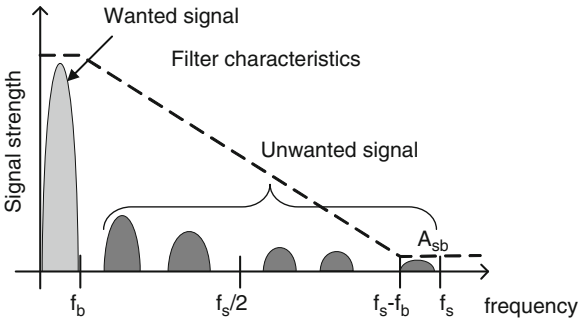

Fig. 7.2 Required characteristics of the analog filter

Table 7.2 Communication standards and filter specification

Standard	f_b (MHz)	Min att. (dB)
Bluetooth	0.7	30 @ 1.5 MHz
UMTS TDD	0.7	63 @ 3.84 MHz
UMTS FDD	2.5	58 @ 11.9 MHz
DVB-H	4.0	49.8 @ 19.8 MHz
WLAN 802.11a	10.0	49.8 @ 48.6 MHz
WLAN 802.11n	20.0	49.8 @ 96.6 MHz

where N_p is the order of the Butterworth filter. Therefore,

$$-A_{SB,dB}(f_s - f_b) \approx -20N_p \log\left(\frac{f_s - f_b}{f_b}\right) - A_{p,dB} \tag{7.2}$$

Serving (7.2), we can get the required filter order N_p.

$$N_p \geq \frac{A_{SB,dB}(f_s - f_b) - A_{p,dB}}{20\log\left(\frac{f_s - f_b}{f_b}\right)} \tag{7.3}$$

The required specifications above for analog filters still vary widely with respect to communication standards and ADC characteristics, such as the roles division between digital filters and analog filters and the sampling frequency. To grasp an image, we summarize various communication standards and the required minimum attenuation for Butterworth filter which is used in signal band in Table 7.2 [1].

According to the above function, for signal bandwidth from 0.7 to 20 MHz, the required filter order is about 4^{th} or 5^{th}. The noise of generic filters is from 50 to 80 μVrms and IIP3 from 16 dBm to 20 dBm.

Higher order filter is necessary with lower sampling frequency. Assuming that the filter order is 4^{th}, the required sampling frequency is about five times as higher as the signal bandwidth. Therefore, with signal bandwidth of 20 MHz, the required minimum sampling frequency is 100 MHz, while the minimum sampling frequency increases to 200 MHz for 40 MHz signal bandwidth.

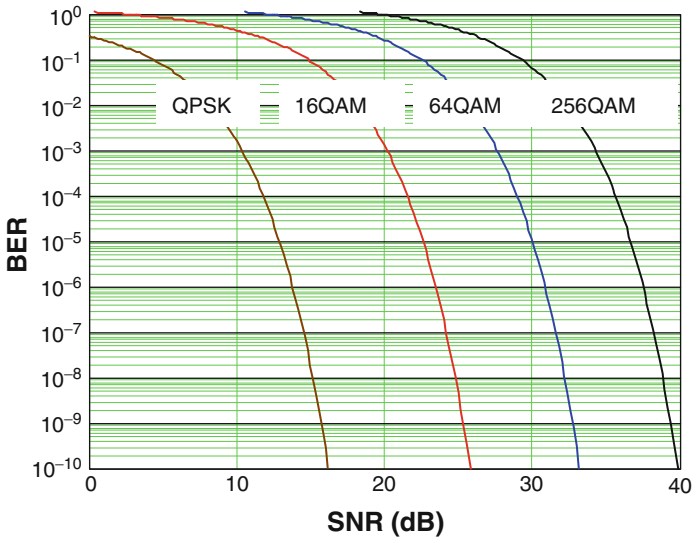

Fig. 7.3 BER versus SNR of various modulation methods

7.2.3 Resolution

In practice, the necessary resolution of an ADC is determined by the required signal-to-noise ratio (SNR) to ensure a reasonable low bit error rate, the level of unwanted signals and the SNR degradation allowed by the ADC. Digital modulation techniques like n-phase phase shift keying (PSK) or n-level QAM are often used in wireless communication. For n-phase PSK or n level QAM, the bit error rate (BER) can be expressed as:

n-PSK:

$$BER \approx erfc\left(\sqrt{SNR}\sin\frac{\pi}{n}\right) \tag{7.4}$$

n-QAM:

$$BER \approx 2\left(1-\frac{1}{\sqrt{n}}\right)erfc\left(\frac{\sqrt{2SNR}}{2\left(\sqrt{n}-1\right)}\right) \tag{7.5}$$

Figure 7.3 shows the plot of BER versus SNR. The required minimum BER is different with different error correction techniques. To obtain a BER of 10^{-3}, the required SNR is about 10 dB for QPSK, 20 dB for 16 QAM and 28 dB for 64 QAM.

The SNR mentioned above should be kept even when both the desired signal and interfering signals (i.e. blocker) enter an ADC at the same time.

For example, Fig. 7.4 shows the wanted signal, unwanted signal, thermal noise and quantization noise for DCS-1800 and WCDMA system. For DCS-1800 system, due to the narrow signal band, filters do not suppress the blocker less than the desired signal. Therefore, the required SNR of the ADC is about 86 dB. However,

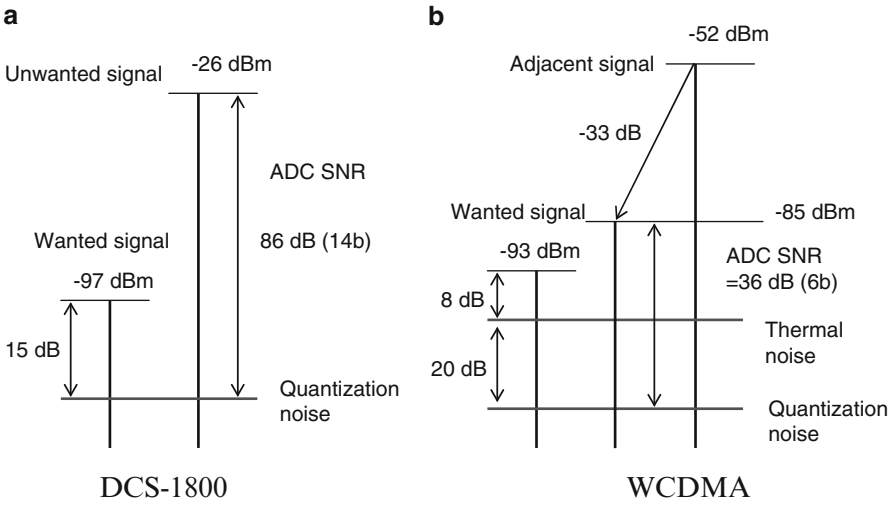

Fig. 7.4 Level of wanted signal, unwanted signal, thermal noise and quantization noise for DCS-1800 and WCDMA system

for WCDMA system, as the filter suppresses the blocker as small as the desired signal, the required SNR of the ADC is decreased to 36 dB.

For an ideal ADC with resolution bit N, oversampling frequency f_s and signal bandwidth f_b, the SNR can be expressed as

$$SNR\,(dB) \approx 6N + 1.8 + 10\log\left(\frac{f_s}{2f_b}\right) \tag{7.6}$$

Normally, the quantization noise of ADC is required to be lower than the thermal noise which is determined by BER. With thermal noise power, P_{th}, and quantization noise power, P_q, SNR (dB) degradation due to ADC quantization noise ΔSNR is given by

$$\Delta SNR(dB) = 10\log\left(1 + \frac{P_q}{P_{th}}\right) \tag{7.7}$$

To limit the degradation to about 0.2 dB, $\frac{P_q}{P_{th}} < 0.047$ must be satisfied. It is required that the SNR of the ADC should be 13 dB higher than that determined only by the thermal noise. In other word, the resolution of the ADC needs to be improved by 2 to 3 bits.

7.3 Delta-Sigma $(\Delta\Sigma)$ ADC

The current multi-standard core ADCs for mobile phones and wireless LANs are ΔΣ ADCs [2–4]. Successive approximation (SAR) ADCs and pipeline ADCs have also been considered as a candidate. However, although SAR ADCs consume low

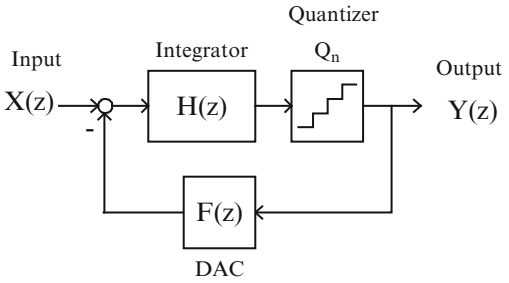

Fig. 7.5 Block diagram of a first order delta-sigma ADCs

power, the SNR of SAR ADCs is only about 60 dB, which makes it unsuitable for multiband receivers which require SNR better than 70 dB. Furthermore, the sampling frequency of SAR ADCs usually is about 50 MSps, which indicates that SAR ADCs can only handle signal bandwidth to an extent of 10 MHz. On the other hand, pipeline ADCs can realize 200 MSps sampling frequency and are suitable for wideband signal. However, the SNR of pipeline ADCs is also limited to about 65 dB. Therefore, the application of pipeline ADCs for multiband receivers which need SNR better than 70 dB is restricted.

In the following, we will simply describe the principle of ΔΣ ADCs, as mentioned above, which are the core ADCs of multi-standard type ADCs.

The basic block diagram of the ΔΣ ADC is shown in Fig 7.5. The entire system is configured as a negative feedback circuit. The output of the quantizer is converted to an analog signal by the feedback DAC circuit, and subtracted from the input signal. Then the differential signal is integrated onto the integrator and quantized by the quantizer. With the input signal X(z), the integrator transfer function H(z), the feedback transfer function F(z) and quantization noise Q_n, the output function Y(z) are expressed as

$$Y(z) = \frac{H(z)}{1+H(z)F(z)}X(z) + \frac{1}{1+H(z)F(z)}Q_n \tag{7.8}$$

The absolute value of the feedback transfer function F(z) is about 1 in signal bandwidth. If F(z) is chosen to be nearly flat, since the absolute value of the integrator transfer function H(z) is designed to be much larger than 1, (7.8) can be approximated as

$$Y(z) = \frac{1}{F(z)}\left\{X(z) + \frac{1}{H(z)}Q_n\right\} \tag{7.9}$$

Thus, from (7.9) we know that the output of Analog-to-Digital conversion is proportional to the input signal while the quantization noise is reduced by a factor of $|H(z)|$. Now, considering a first-order integrator with the simplest configuration and F(z) shifted by one clock,

$$\begin{aligned} H(z) &= \frac{1}{1-z^{-1}} \\ F(z) &= z^{-1} \end{aligned} \tag{7.10}$$

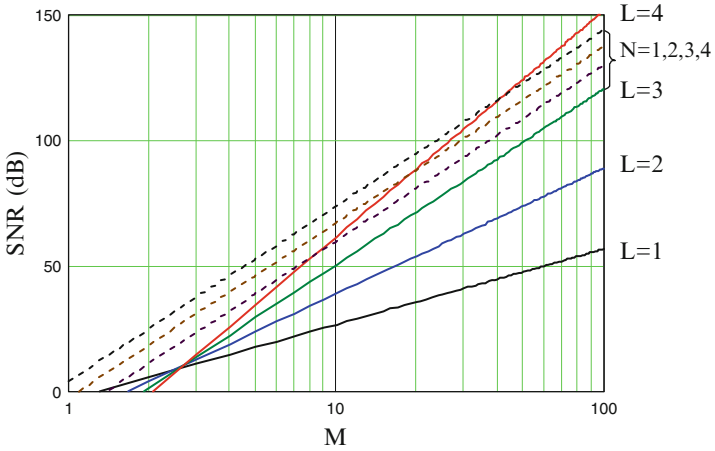

Fig. 7.6 SNR vs. Oversampling Rate M

Substituting it to (7.8), we get

$$Y(z) = X(z) + \left(1 - z^{-1}\right) Q_n \tag{7.11}$$

Where

$$z = e^{j2\pi \frac{f}{fs}} \tag{7.12}$$

Assuming $2\pi \frac{f}{f_s} \ll 1$, then

$$\left|1 - z^{-1}\right| = \left|1 - e^{-j2\pi \frac{f}{fs}}\right| = \left|1 - \cos\left(2\pi \frac{f}{f_s}\right) - j\sin\left(2\pi \frac{f}{f_s}\right)\right| \approx \left|2\pi \frac{f}{f_s}\right| \tag{7.13}$$

From (7.13) we see that the low frequency component of the quantization noise is suppressed.

With an N-bit quantizer, L-th order filter, and oversampling ratio of $\mathrm{M} = \frac{f_s}{2f_b}$, the SNR is expressed as below.

$$SNR = \frac{3\pi}{2}\left(2^N - 1\right)^2 (2L+1)\left(\frac{M}{\pi}\right)^{2L+1} \tag{7.14}$$

Figure 7.6 shows the plot of the SNR versus oversampling ratio when the filter order L is from 1 to 4 for the single-bit quantizer and when the number of the bit N is from 1 to 4 for L equal to 3.

As can be seen from Fig. 7.6, the SNR of ΔΣ ADCs can be improved by increasing the oversampling ratio in the same configuration. Even with the same oversampling ratio, for the narrower band signal the higher SNR can be achieved,

while for wide bandwidth signal SNR naturally decreases. As a result, it is easy to support multi-standard applications. In fact, ΔΣ ADCs are utilized in most of multi-standard ADCs.

7.4 Basic Block Diagram of Delta-Sigma ADCs

As shown in Fig. 7.7, there are two types of ΔΣ ADCs according to the construction of the integrator, (a) DT (Discrete Time) ΔΣ ADC using switched-capacitor integrator and (b) CT (Continuous Time) ΔΣ ADC using continuous-time integrator. In CT ΔΣ ADC, the distortion of the sample-and-hold (S/H) circuit is suppressed because it is in the negative feedback loop.

Furthermore, CT ΔΣ ADC is suitable for wide bandwidth signal because the bandwidth of the integrator can be easily widened. Compared to DT ΔΣ ADC, it can realize lower power consumption. Since anti-aliasing filter is built-in CT ΔΣ ADC, it is applicable for wireless communications without the need for an additional anti-aliasing filter before the ADC. However, the accuracy of CT ΔΣ ADC is deteriorated significantly by the timing-jitter of clock applied to the built-in DAC. Also it is necessary to adjust the time constant of the integrator. Another issue is that CT ΔΣ ADC is inclined to be unstable because it is easily affected by the excess loop delay of the comparator. In fact, in DT ΔΣ ADC, at least in the first-stage,

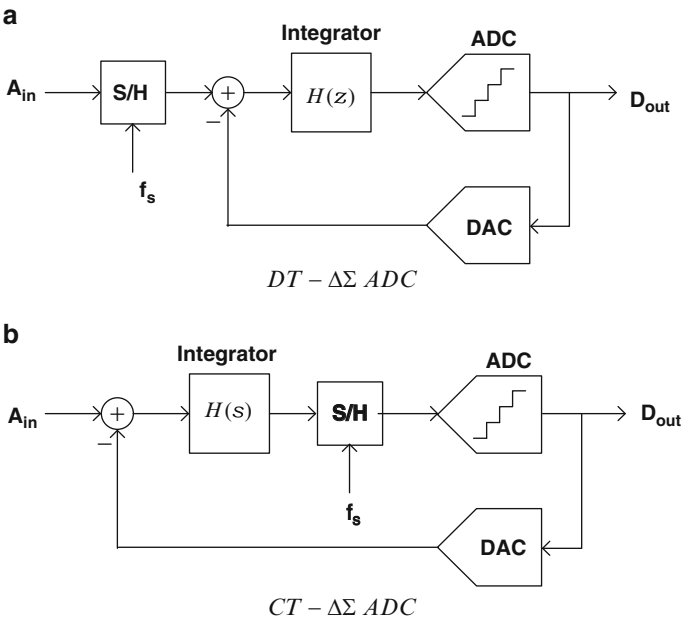

Fig. 7.7 Structure of discrete-time and continuous-time sigma-delta ADC

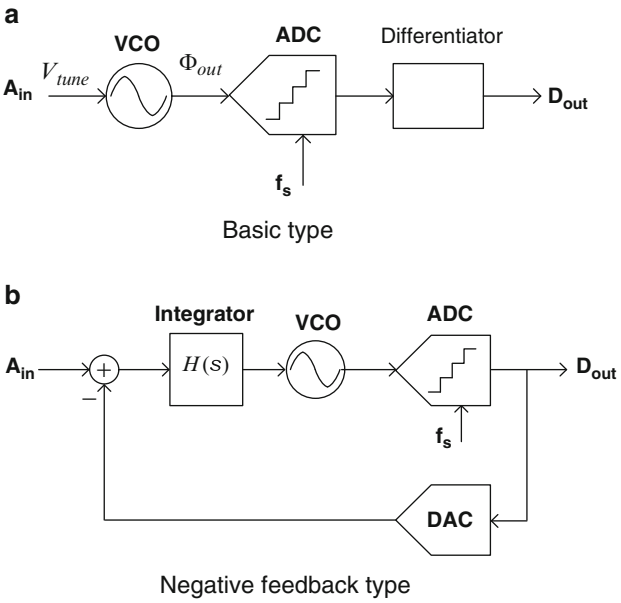

Fig. 7.8 ΔΣ ADCs by using VCOs

operational amplifier integrator is necessary. The ratio between signal bandwidth and sampling frequency is high because the oversampling ratio is at least 8, so it is easy to implement the anti-aliasing filter before the ADC. Therefore there is almost no significant difference for CT ΔΣ ADC and DT ΔΣ ADC.

Recently ΔΣ ADC by using Voltage Controlled Oscillator (VCO) has been attracting more attention. We will introduce it for it is considered useful to realize broadband ΔΣ ADC in the future. Figure 7.8a shows the basic form [5–8] and (b) is a negative feedback structure [9].

The oscillating frequency of the VCO is proportional to the control voltage. The phase is the time integration of the frequency. Therefore, the transfer function between the output phase, Φ_{out} and the control voltage, V_{tune} is given by

$$\Phi_{out} = \frac{K_{VCO}}{S} V_{tune} \tag{7.15}$$

As can be seen from (7.15), the transfer function is a first-order integration. The circuit shown in Fig. 7.8a forms a first-order ΔΣ ADC. The integrator used in the VCO differs from normal integrators. Its output does not saturate, therefore it can achieve a perfect integration. Since it can be easily achieved by multi-stage ring oscillators and flip-flops, the phase quantizer is suitable for integration.

However, the issue of this simple method is poor linearity and large distortion. Figure 7.8b shows a negative feedback type ΔΣ ADC. By using negative feedback, the distortion due to the nonlinearity can be suppressed by large loop gain. Usually a second-order or third-order integrator is often used in the negative feedback loop.

7.5 Delta-Sigma ADCs for Multi-Standard Applications

As a reference, Fig. 7.9 shows the relationship between the SNR and signal bandwidth f_b of ΔΣ ADCs recently developed for multi-standard ADCs [8–17].

As shown in Fig. 7.9, the SNR and signal bandwidth tends to be inversely related. With the signal power, P_S, noise power spectral density, P_N/H_Z, and signal bandwidth, f_b, SNR can be expressed as

$$SNR(dB) = 10\log\left(\frac{P_S}{P_N/Hz}\right) - 10\log f_b = SNR_0(dB/Hz) - 10\log f_b \qquad (7.16)$$

SNR_0 (dB/Hz) is denoted by the first term on the right side of the equation when f_b is equal to 1 Hz. In most case SNR_0 is from about 135 dB/Hz to 143 dB/Hz. But at f_b = 20 MHz, there are two ΔΣ ADCs which achieve 150 dB/Hz SNR_0 (dB/Hz) [9, 10].

SNR_0 is related closely to CMOS technology node. Figure 7.10 shows the relationship between technology nodes and noise floor of ADCs published in the year 2010 [18]. To achieve a 143 dB/Hz SNR_0, it is necessary to use 65 nm technology node or less advanced ones. And it is difficult to achieve this value for more advanced technology nodes. Of course, the low maturity of advanced CMOS technology causes high noise floor. Even if the technology has matured, due to the tendency that the achieved SNR_0 becomes lower as CMOS technology scales down, it becomes difficult to achieve high SNR.

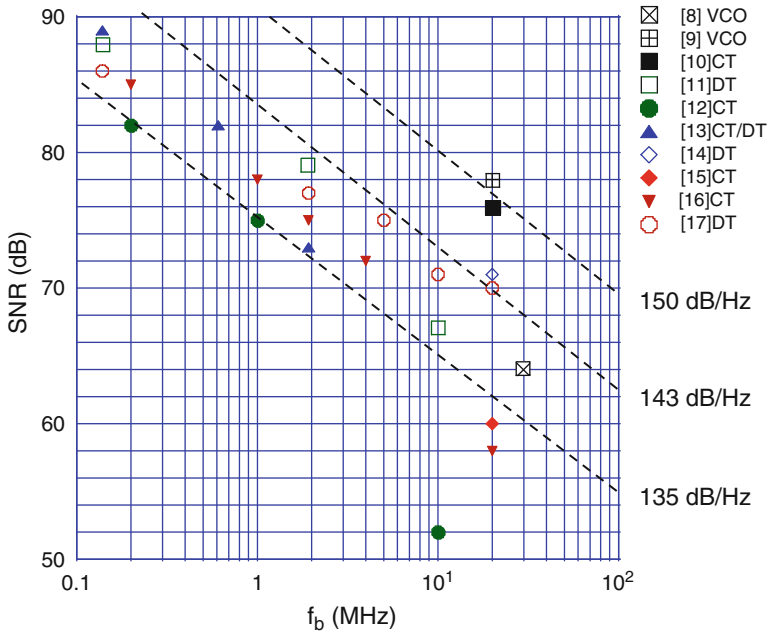

Fig. 7.9 SNR virus signal bandwidth f_b of ADCs for multi-standard applications

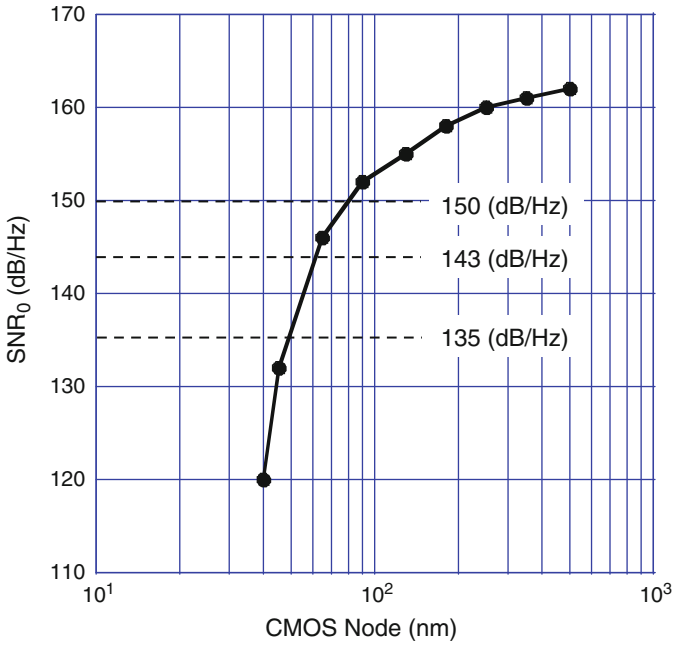

Fig. 7.10 SNR_0 versus CMOS technology node for ΔΣ ADCs

From Fig. 7.9 we note that below 10 MHz, CT and DT ΔΣ ADC has little difference in performance other than that DT ΔΣ ADC has a slightly higher SNR. In general, it is said that as the signal frequency becomes higher, CT ΔΣ ADCs become more advantageous. However, even though above 10 MHz, the CT ΔΣ ADC in [10] achieves high SNR; the performance of some of CT ΔΣ ADCs is significantly degraded and DT ΔΣ ADCs achieve higher SNR [14, 17]. ΔΣ ADCs using VCOs show the best SNR at 20 MHz [9] and achieve a wide bandwidth of 30 MHz [8]. It is worthy of studying ΔΣ ADCs using VCOs for broadband signal in future.

In the following we will discuss performance limitations of ΔΣ ADCs.

7.5.1 Resolution, Order and Sampling Frequency

With the sampling frequency f_s, and signal bandwidth f_b, the SNR function given by (7.14) can be expressed as

$$SNR = \frac{3\pi}{2}\left(2^N - 1\right)^2 (2L+1)\left(\frac{f_s}{2\pi f_b}\right)^{2L+1} \tag{7.17}$$

where N is the resolution bit and L is the number of order.

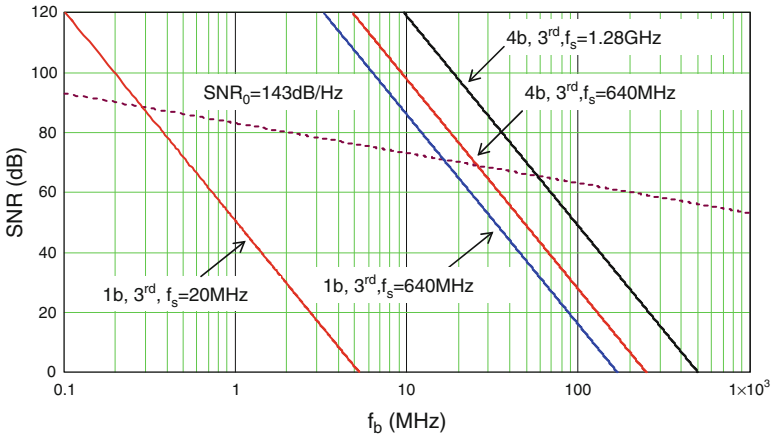

Fig. 7.11 SNR under various parameter variables

Based on (7.17), the plots of the SNR with various parameter variables are shown in Fig. 7.11. As performance criteria the line of SNR equal to 143 dB/Hz is also plotted. To ensure the stability, the order of the filter is generally 3rd or 4th order. In Fig. 7.11 we give the SNR with a 3rd order filter. The resolution of ΔΣ ADCs is maximally 4 bits considering the quantizer driver, circuit scale and the resolution of DACs. Currently the maximum over-sampling frequency for wideband ΔΣ ADCs is about 640 MHz. Therefore, with this value, for a 20-MHz bandwidth signal the SNR is about 78 dB. If the same SNR is achieved for a 40-MHz bandwidth signal, the over-sampling frequency should increase up to 1.28 GHz.

However, the noise resulting from DAC's mismatch in ΔΣ ADCs is not shaped. By employing dynamic element matching (DEM), the first-order noise-shaping can be implemented for DAC's mismatch. Consequently, the effect of the mismatch is significantly alleviated. Nevertheless, for wideband signal ΔΣ ADCs, the SNR is limited from 75 dB to 80 dB due to this mismatch. To obtain higher SNR, a single-bit quantizer and DAC are necessary. For a single-bit 3rd-order ΔΣ ADC with a sampling frequency of 640 MHz, the maximum signal bandwidth is about 15 MHz with an SNR over 143 dB/Hz. Therefore, for signal bandwidth less than 15 MHz the necessary SNR can be achieved with a single-bit quantizer. Compared to multi-bits quantizer, it is at the cost of high sampling frequency, high signal bandwidth of the operation amplifier and large power consumption. Additionally, for single-bit quantizer, the integrator tends to saturate and thus the dynamic rang declines. Normally, single-bit ΔΣ ADCs are employed for signals with bandwidth less than 1 MHz. Moreover, for low frequency band, sufficiently high SNR can be obtained even at lower sampling frequency. For example, for signal bandwidth below 300 kHz, a single-bit, 3rd-order ΔΣ ADC can achieve an SNR as high as about 90-dB at 20-MHz sampling frequency.

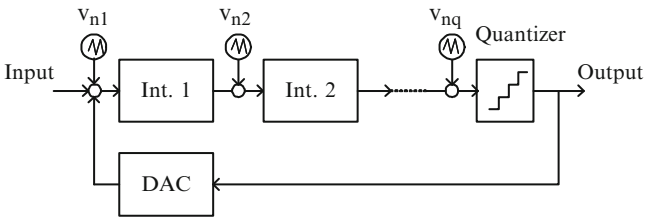

Fig. 7.12 Noise sources of the ΔΣ ADC

7.5.2 Noise Effect

As given in (7.14), the effect of the quantization noise of the ΔΣ ADC can be reduced with the increase of the integrator order, L, and over-sampling ratio, M. However, noises from other source still need to be considered.

Figure 7.12 shows noise sources of the ΔΣ ADC. v_{n1} represents the equivalent input-referred noise of the first integrator. For DT ΔΣ ADCs it is the sampling noise, while for CT ΔΣ ADCs it includes the resistor noise, DAC noise and so on. v_{n2} represents the equivalent input noise of the second integrator and v_{nq} is the quantization noise. The circuit equivalent input noise v_{ni} is given by

$$v_{ni}^2 = \frac{1}{M}\left\{v_{n1}^2 + \frac{v_{n2}^2}{3}\frac{1}{A_2^2}\left(\frac{\pi}{M}\right)^2 + \cdots + \frac{v_{nq}^2}{2i+1}\frac{1}{A_i^2}\left(\frac{\pi}{M}\right)^{2(i-1)}\right\} \tag{7.18}$$

where A_i is the gain of the i^{th} integrator. If

$$\frac{1}{3}\left(\frac{\pi}{A_2 M}\right)^2 \ll 1, \tag{7.19}$$

v_{n1} will dominate the ADC noise. Since the gain of the first integrator is about from 0.2 to 0.3, with M greater than 32, v_{n1} will totally dominate the ADC noise. If M is less than about 16, the noise of the second integrator should also be considered.

Now, assuming v_{n1} dominates the entire noise and it mainly comes from the sampling circuit. Figure 7.13 shows the sampling circuit of the DT ΔΣ ADC. The thermal noise power for a differential sampling circuit is

$$v_n^2 = \frac{2kT}{C_s} \tag{7.20}$$

With the peak-to-peak voltage V_{pp} of a sine wave, the SNR is given by

$$SNR\,(dB) = 10\log\left(M\frac{C_s V_{pp}^2}{16kT}\right) \tag{7.21}$$

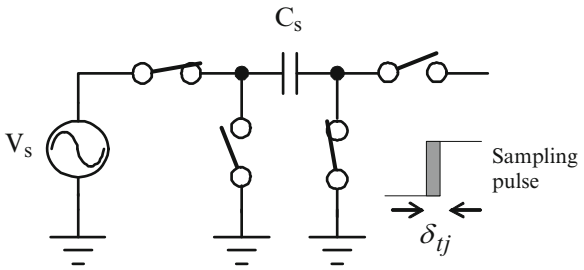

Fig. 7.13 Sampling circuit of the DT ΔΣ ADC

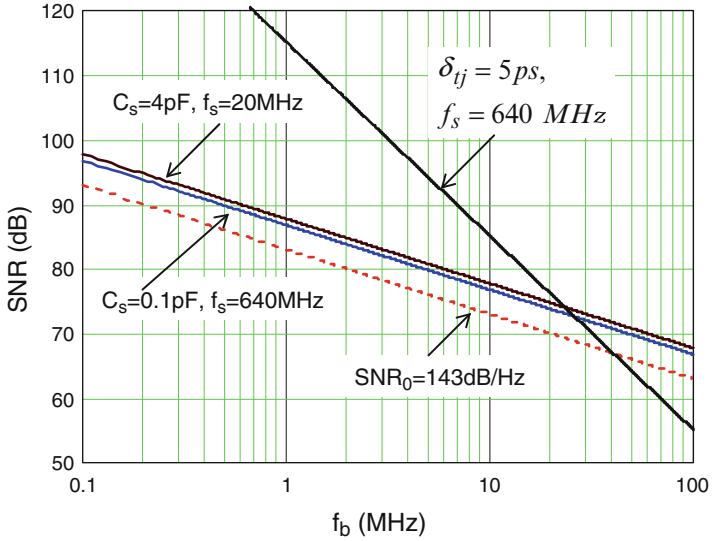

Fig. 7.14 SNR versus signal bandwidth f_b with sampling noise and sampling jitter noise

Since the noise of the sampling circuit is resulting from the sample timing jitter. The SNR can be expressed as

$$SNR\,(dB) = 10\log\left(\frac{M}{(2\pi f_b \sigma_{tj})^2}\right) = 10\log\left(\frac{f_s}{2f_b^3\,(2\pi\sigma_{tj})^2}\right) \tag{7.22}$$

where σ_{tj} is the standard deviation of the sample timing jitter.

Figure 7.14 shows the SNR with sampling noise and sampling jitter noise. Increasing the signal bandwidth f_b will decrease the oversampling ratio M. Consequently, SNR will decrease at a slope of -10 dB/dec under constant sampling capacitance. Nevertheless, if the noise floor doesn't change, the required SNR for ADCs has the same slope. Therefore, it is better to use constant sampling capacitance for constant sampling frequency. However, in order to save power for small signal bandwidth, it is better to reduce the sampling frequency. In this case,

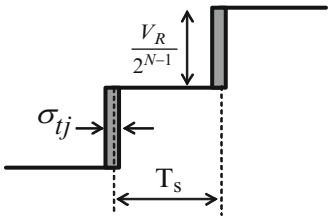

Fig. 7.15 Timing jitters of the DAC and the fluctuation of generated signals

for low oversampling ratio, we need to increase the sampling capacitance further to decrease the noise floor. For example, when $f_s = 640\,\text{MHz}$, it is better to have a $0.1 - \text{pF}$ sampling capacitance, while about $3.2 - \text{pF}$ sampling capacitance is necessary with f_s of 20 MHz.

From (7.22) we can see that the sampling jitter noise is proportional to the cube of the signal bandwidth. Thus the SNR rapidly degrades with increasing signal bandwidth as shown in Fig. 7.14. This the main reason for SNR degradation at tens MHz bandwidth. For $f_s = 640\,\text{MHz}$ and $f_b = 20\,\text{MHz}$, the standard deviation of the sample timing jitter is required to be less than 5 ps to obtain an SNR above 75 dB. As a result not only the performance of the ADC but also the performance of the PLL needs to be improved.

Moreover, for the CT ΔΣ ADC there is noise generated from the sample timing jitter of the DAC. The sampling pulse under clock jitter influence is shown in Fig. 7.15 where N is the resolution bit of the DAC and σ_{tj} is the standard deviation of the sample timing jitter.

Assuming the oversampling ratio M is large enough and the nonlinearity of the DAC is limited to 1LSB, the induced noise power P_n is

$$P_n = \left(\frac{V_R}{2^{N-1}} \frac{\sigma_{tj}}{T_s} \right)^2 \tag{7.23}$$

With the signal power $P_s = \frac{V_R^2}{8}$, SNR can be expressed as

$$SNR\,(dB) = 10\log\left\{ \frac{V_R^2}{8} \frac{2^{2N-2}}{V_R^2} \frac{T_s^2}{\sigma_{tj}^2} M \right\} \tag{7.24}$$

and simplified as

$$SNR\,(dB) = 10\log\left\{ \frac{2^{2N}}{64} \frac{1}{\sigma_{tj}^2 f_s f_b} \right\} \tag{7.25}$$

From (7.25) we know that the SNR is proportional to the resolution bit N, while inversely proportional to the sampling frequency, signal bandwidth and the quadratic power of the timing jitter. Thus it becomes difficult to achieve the predetermined SNR at high sampling frequency and with large timing jitter without increasing the resolution bit of the DAC, as shown in Fig. 7.16.

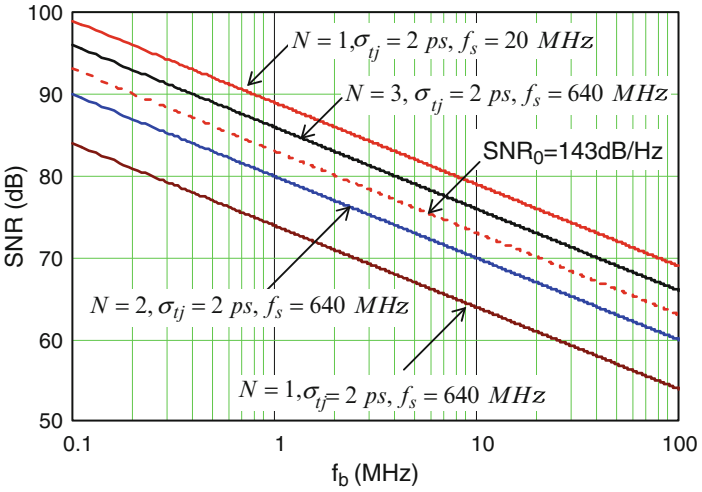

Fig. 7.16 SNR versus signal bandwidth f_b under the timing jitter influence of DAC

Due to the timing jitter, the SNR degrades with a slope of 10 dB/dec for constant signal bandwidth. Increasing the resolution bit of the DAC can alleviate the effect of the timing jitter. However, with the concern of the comparator drive and implementation of the DAC, it is better to have the resolution bit of 4. To realize an SNR above 80 dB it is necessary to use single-bit DACs. With the concern for the timing jitter, we can reduce the sampling frequency. The effect of the DAC jitter is more serious for the CT ΔΣ ADC. Especially for wideband signals, to realize a high SNR, the oversampling ratio needs to be as high as possible to alleviate the effect of quantization noise and sampling noise. Higher oversampling ratio means higher sampling frequency or shorter sampling period and then CT ΔΣ ADCs become more susceptible to jitter. Jitter level is determined by the PLL and the improvement is limited. Thus, even though it is believed that CT ΔΣ ADCs are applicable for wideband signals, timing jitter is considered as the main limitation for its usage.

7.5.3 Signal Bandwidth and Power Consumption

Figure 7.17 shows the power consumption versus signal bandwidth.

The power consumption of the published ADCs has a tendency as

$$P_d\,(mW) = K\sqrt{f_b(MHz)} \tag{7.26}$$

where K is about 2.5 ∼ 8. Generally CT ΔΣ ADCs have low power consumption. At $f_s = 20$ MHz, CT ΔΣ ADCs consume low power [15, 16] but the SNR is below

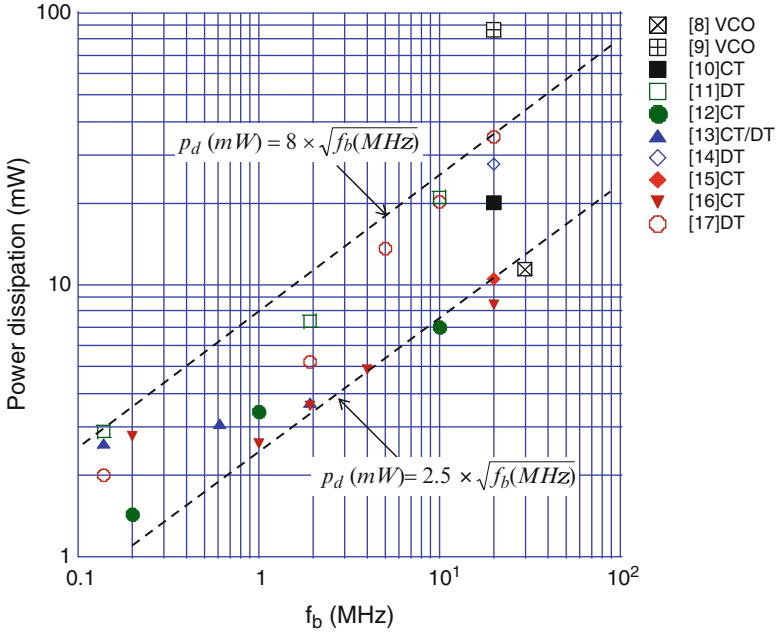

Fig. 7.17 Power consumption versus signal bandwidth

60 dB. While DT ΔΣ ADCs have an SNR over 70 dB. Thus they can not be compared directly. The ΔΣ ADC with a VCO in [9] has a power consumption of 87 mW, which is so large and out of the region between the trend lines. At $f_s = 20$ MHz it realize a 78 dB SNR, so the power consumption is a little large. However, from the view of a CT ΔΣ ADC with a power consumption of 20 mW in [10] which realizes almost the same SNR, the power consumption is considered to be too large and it seems to be necessary to optimize the circuit. It is notable that the ΔΣ ADC with a VCO in [8] achieves a 30-MHz signal bandwidth, a reasonable SNR of 64 dB and a low power consumption of 11 mW.

7.6 Digital-to-Analog Converters (DAC)

As shown in Fig. 7.18, to suppress the aliasing, a filter is necessary after DAC for transmitters. For multiband transmitters the main method is to switch the bandwidth of the filter. The frequency of aliasing signals increases with increased sampling frequency of the DAC. Thus even with a low order filter the aliasing signals can be effectively eliminated. For this reason, the sampling frequency is set to be more than four times as high as the symbol rate.

The DAC shown in Fig. 7.19 employs current arrays. Usually, the upper bits, about 4 to 6 bits, are unary weighted and the lower bits are binary weighted. Area

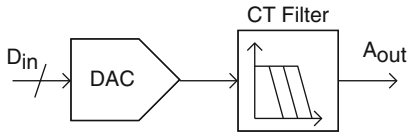

Fig. 7.18 Digital to analog converter and continuous time filter for receivers.

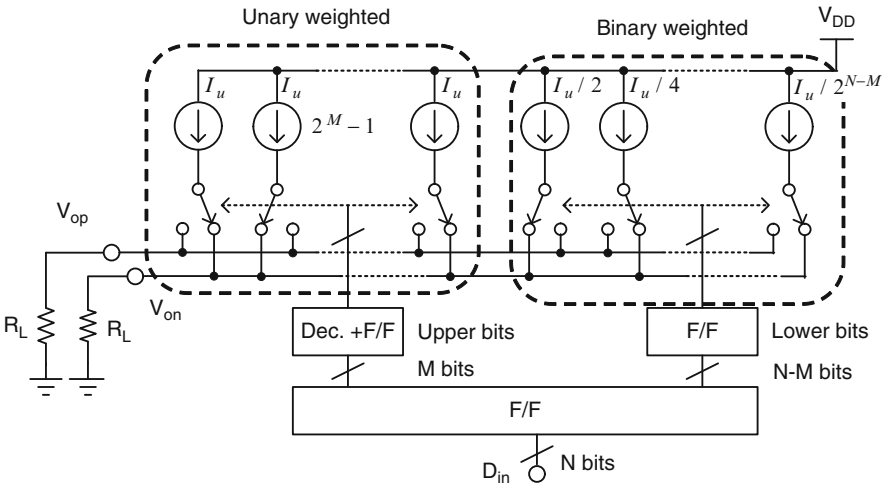

Fig. 7.19 Digital to analog converter with current array

and accuracy can be well-balanced with such a configuration. For 64 QAM modulations the required accuracy can be achieved by a current source based 12-bit DAC without any special linearity calibration circuit. While for 256 QAM modulations, a 14-bit DAC is necessary and it should need the linearity calibration circuit.

For DACs, it is easy to have a sampling frequency above 1 GHz and the speed is high enough for commonly-used wireless communications. Since the power consumption is nearly determined by the signal swing and load resistance, increasing the load resistance at low data rate can reduce the current and save power without compromising the circuit performance.

However, the issue of this type DAC is that the load impedance decreases with increasing number of parallel current sources connected to the load. Since the number of the parallel current source varies with input code, the load impedance will change with input signals and thus the non-linearity increases for high frequency. The effect is not remarkable for signal frequency less than 10 MHz; however when signal frequency above 100 MHz, it becomes noticeable. Several methods have been proposed to reduce this effect [19].

Another way of implementing DAC or maybe the way to render the conventional DAC unnecessary is to use all-digital transmitter described in Chap. 3. Power mixer array, which is presented in the next chapter, has some part of DAC functionality, and required number of bit can be reduced (however it requires higher sampling rate).

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Chapter 8
Highly Linear and Efficient Watt-Level SDR Transmitter with Power Mixer Array

Shouhei Kousai

8.1 Introduction

The main challenge for the SDR transmitter is to realize highly flexible and programmable power amplifier (PA) as well as highly power and area efficient PA, which is usually the most power and area consuming building block in a transceiver. A conventional IQ transmitter consists of many analog and RF building blocks, as depicted in Fig. 8.1. Matching networks are tuned to a fixed frequency band to maximize the power and area efficiency for an existing standard, offering little flexibility. Another issue is the poor power efficiency of class-AB power amplifiers used in a conventional transmitter. This issue should be emphasized with CMOS implementations which further degrades the power efficiency, as they are essential for a future one-chip and low-cost SDR.

One way to solve the problem is to employ digital polar architecture described in Chapter 3. The phase modulated local oscillator (LO) signal, which is generated by an all-digital PLL, is multiplied with digital envelop signal at a digital PA, creating arbitrary modulated signal at RF as shown in Fig. 8.2. It offers high flexibility as the major building blocks of all-digital PLL and digital PA can be controlled by digital envelope and phase signals which are generated by a digital baseband (BB) circuit. In a scaled CMOS technology, inverters can be employed to buffer and amplify the phase modulated signal, removing the non-flexible, area consuming matching networks. The digital PA has potentially high power efficiency, as switching amplifier units are employed [1–3].

However, there are several issues for the digital polar architecture when it is applied to a high power, watt-level transmitter. First, since the envelope signal is reconstructed with discrete levels, quantization noise is produced and aliasing

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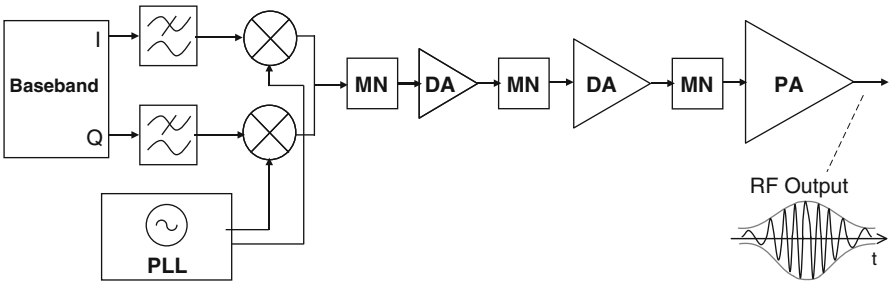

Fig. 8.1 The block diagram of a wideband direct conversion IQ transmitter

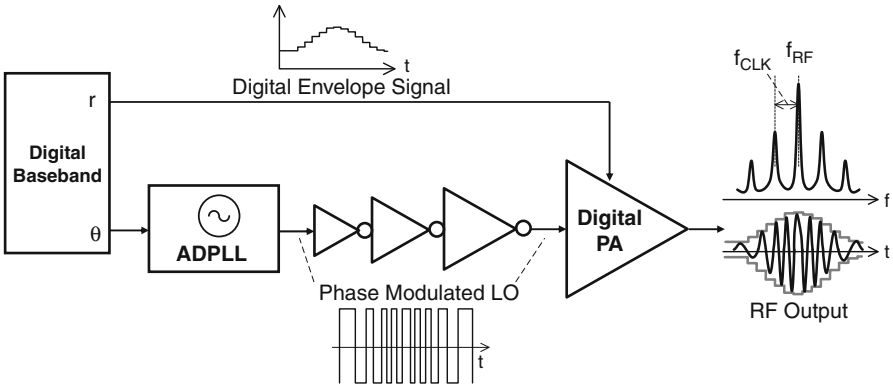

Fig. 8.2 The block diagram of an all digital polar transmitter

signal are observed at $f_{RF} +/- f_{CLK}$, $f_{RF} +/- 2f_{CLK}$, $f_{RF} +/- 3f_{CLK}$…. As they are created at the output of a transmitter, it is difficult to suppress them below the acceptable level, where they do not interfere other wireless communication networks. Although several ways are proposed to minimize the quantization noise and alias signal, power efficiency and occupied area must be sacrificed. Second, due to the feed through issue [4, 5], small output power, which is required with most of the cellular standards, cannot be generated without power and area consuming additional RF gain control circuits. This is also an issue when the modulated signal has large peak-to-average power ratio, OFDM signals for example. Third, reported power efficiency is not as high as expected especially with high output power levels. The reason might be the difficulty to realize power efficient layout, which is critical to the watt-level power amplifier, as a lot of power amplifier units have to be placed and wirings from unit amplifier to the output have to have equal length for the accurate modulation.

8.2 Power Mixer Array Transmitter Subsystem

8.2.1 Architecture

In order to overcome the challenges described in Sect. 8.1, we propose the power mixer array transmitter subsystem, whose basic concept is illustrated in Fig. 8.3 [6]. Power generation and amplitude modulation are done by several identical up-conversion power mixer units. The inputs of power mixer units are a BB envelope signal and phase modulated LO signal. A switching power mixer described in Sect. 8.3.2 can be utilized to obtain high peak efficiency. The power mixer array provides large output power range without any need for RF gain control, as we will explain in Sect. 8.4. Therefore, simple digital gates (e.g., inverters) can be used to buffer the identical phase modulated LO and then applied to the power mixer units, resulting in a small die area and low power consumption. On the other hand, different BB input signals can be applied to each power mixer unit, in general. The output currents of the mixers are directly combined at their output. It should be noted that the power mixer array also subsumes some of the blocks typically implemented on a transmitter chip (e.g. driver amplifiers with matching network), rendering them unnecessary.

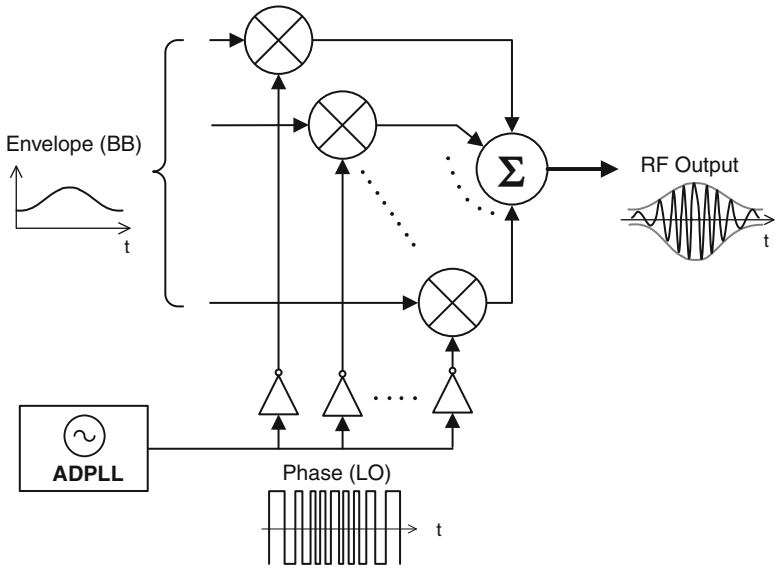

Fig. 8.3 The basic concept of power mixer array architecture

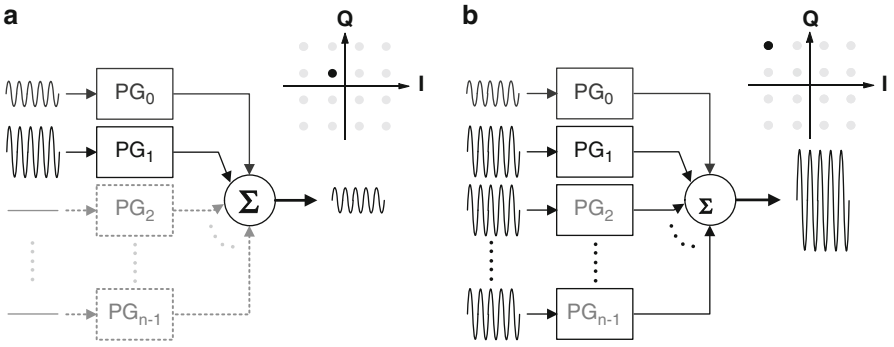

Fig. 8.4 Segmented power generation scheme with (**a**) small output power, and (**b**) large output power

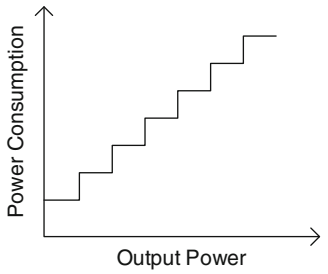

Fig. 8.5 Power consumption of the segmented power generation scheme

8.2.2 Segmented Power Generation

In this section, the advantages of the *segmented power generation* scheme, in which power is generated by several identical units, is explained. The basic operation of the segmented power generation scheme is depicted in Fig. 8.4. When a symbol requires a small output power as shown in Fig. 8.4a, most of the power generation units (PG) can be turned off and the power is generated by only a few units, where one of the units is operating at intermediate power levels to produce continuous output power levels and the remaining ones are operating either at full power or off. Figure 8.4b describes the operation when a symbol requires a large output power. The operation of the first power generation unit remains the same, as it produces intermediate power levels, while the remaining power generation units are operating at their full power. In the segmented power generation scheme, power consumption is almost proportional to the output power, as shown in Fig. 8.5, and thus the back-off efficiency dependence is as good as a class-B power amplifier. Unlike the digitally modulated polar PA mentioned in Sect. 8.1, the out-of-band emission problems due to the quantization noise and aliasing signal are avoided since continuous output power levels are generated.

Another benefit of the segmented power generation scheme is the associated linearity improvement. For a conventional power generation circuit, where there s only one power generation unit, the output, Y_1, is expressed in terms of normalized input, x. For a third-order memory-less non-linearity system, we have

$$Y_1(x) = \alpha_1 x + \alpha_3 x^3 (-1 < x < 1), \tag{8.1}$$

where we assume α_1 and α_3 are real and x is the ac input signal (e.g., $x = \mathrm{A}_{in}\cos\omega_1 t$.). To understand the segmented power generation scheme, let us consider a system with two power generation units. We assume: (1) Power generation unit is scaled by half. (2) The scaled input as $2x$ is applied to a single power generation unit for $-0.5 < x < 0.5$, and input of 1 is applied to the unit for $0.5 < x < 1$. (3) The other unit will see of the residue in excess of 1 for $0.5 < x < 1$. Then, the output of the two-unit system, Y_2, is expressed as,

$$\begin{aligned} Y_2(x) &= \frac{\alpha_1 (2x-1) + \alpha_3 (2x-1)^3 + \alpha_1 + \alpha_3}{2} (0.5 < x < 1), \\ Y_2(x) &= \frac{\alpha_1 (2x) + \alpha_3 (2x)^3}{2} \ (0 < x < 0.5), \\ Y_2(x) &= -Y_2(-x) \ (-1 < x < 0). \end{aligned} \tag{8.2}$$

By generalizing this idea, for a segmented power generation system which has m power generation units,

$$\begin{aligned} Y_m(x) &= \frac{\alpha_1 (mx-n) + \alpha_3 (mx-n)^3 + n(\alpha_1 + \alpha_3)}{m} \left(\frac{n}{m} < x < \frac{n+1}{m} \right), \\ Y_m(x) &= -Y_m(-x) \ (-1 < x < 0), \end{aligned} \tag{8.3}$$

where $n = 0, 1, 2, \ldots, m-1$, and Y_m is the output power of the system with m power generation units. In general, Y_m is expressed as,

$$\begin{aligned} Y_\mathrm{m}(x) &= \frac{f(\mathrm{m}x - \mathrm{n}\mathrm{A}_0) + f(\mathrm{n}\mathrm{A}_0)}{\mathrm{m}} \left(\frac{n\mathrm{A}_0}{m} < x < \frac{(n+1)\mathrm{A}_0}{m} \right), \\ Y_m(x) &= -Y_m(-x) \ (-\mathrm{A}_0 < x < 0), \end{aligned} \tag{8.4}$$

where

$$f(x) = \alpha_1 x + \alpha_2 x^2 + \alpha_3 x^3 + \ldots, \tag{8.5}$$

and A_0 is the full-scale input amplitude. In (8.4), the maximum input level for a unit is limited to A_0/m. For instance, the calculated output amplitude at frequency ω_1, A_OUT, and gain, $\mathrm{A}_\mathrm{OUT}/\mathrm{A}_\mathrm{in}$ with m of 1, 4, and 16 are plotted in Fig. 8.6, for

$$f(x) = x - 0.63x^3 + 0.23x^5 \tag{8.6}$$

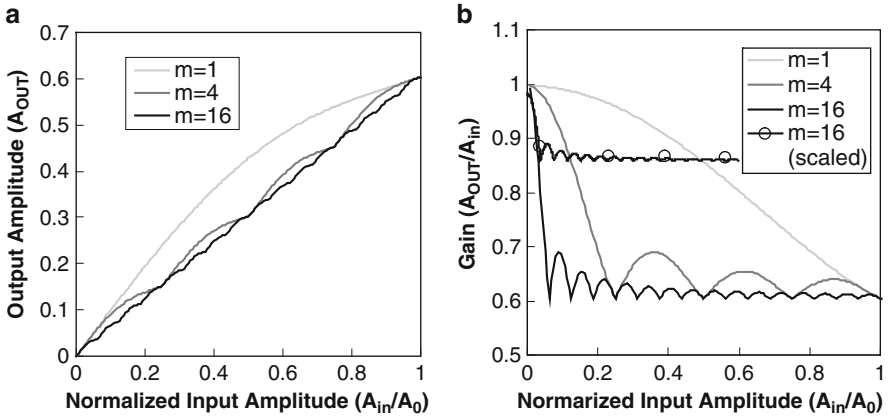

Fig. 8.6 (**a**) The output amplitude and (**b**) gain of the segmented power generation scheme, with m = 1, 4, and 16

and

$$x = \mathrm{A}_{in}\cos\omega_1 t. \qquad (0 < \mathrm{A_{in}} < \mathrm{A}_0) \tag{8.7}$$

where $\mathrm{A_{in}}$ is the input amplitude.

Two interesting phenomena are observed with a large number of power generation unit (m). First, integral nonlinearity (INL) improves, as the output amplitude is almost linearly related to the input amplitude as shown in Fig. 8.6a. Second, the linearity at large signal levels improves substantially, whereas linearity at small signal levels degrades slightly as shown in Fig. 8.6b. This phenomenon can be better understood in the context of inter-modulation distortion (IMD). The IMD product is derived by substituting

$$x = \frac{\mathrm{A}_{in}\left(\cos\omega_1 t + \cos\omega_2 t\right)}{2} \left(0 < \mathrm{A_{in}} < \mathrm{A}_0\right) \tag{8.8}$$

into Eq. (8.6). The output amplitudes of the third order IMD product (IMD_3) at frequency $2\omega_1$–ω_2 or $2\omega_2$–ω_1, are plotted in Fig. 8.7. In a conventional amplifier $(m = 1)$, the IMD_3 product is a cubic function of the input amplitude. However, IMD_3 product with m of 16 is almost linearly related to the input amplitude, resulting in a small distortion at large output power. This *distortion dependence shaping* turns out to be very effective as we consider the power distribution of modulated signals.

To suppress the ripple in terms of gain observed in Fig. 8.6b, two techniques can be employed. First, technique is effective when input amplitude is small. As Eq. (8.4) indicates, the maximum input level of a unit is scaled with the input full-scale amplitude. This guarantees that all of the units operate with full-scale input signal, and the ripple does not have a large impact on the overall linearity.

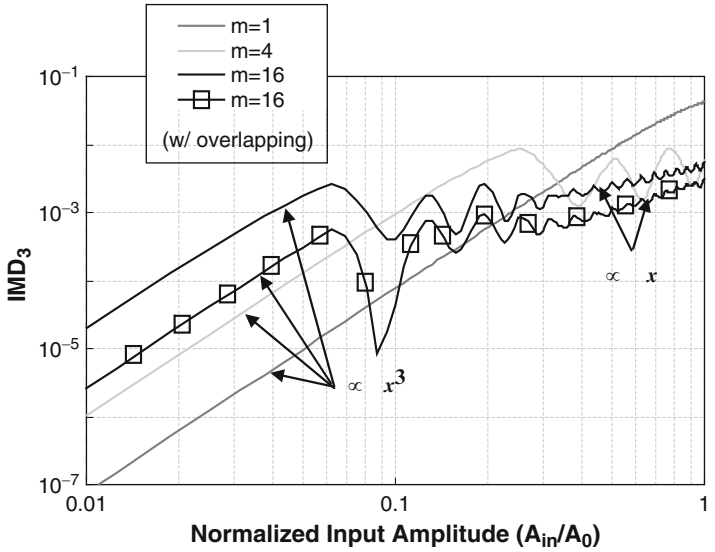

Fig. 8.7 IMD_3 product of the segmented power generation scheme and overlapping

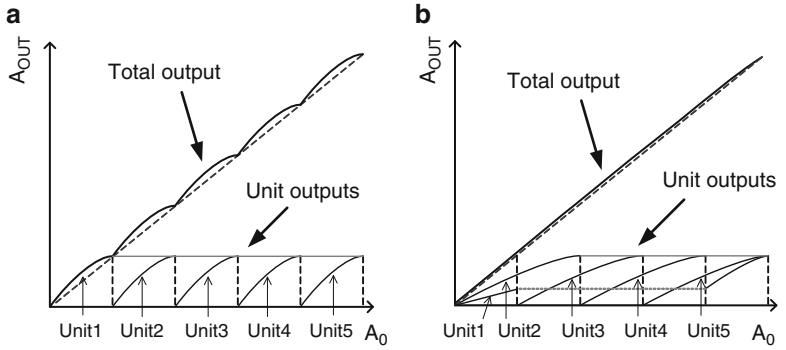

Fig. 8.8 The concept of overlapping technique. (**a**) without overlapping and (**b**) with overlapping

In addition, the unit linearity usually improves as the input level of the unit is decreased. In Fig. 8.4b, the solid line with circle represent the gain when A_0 is scaled to half, where the overall gain flatness is substantially improved from that without scaling. Second approach to improve this even further is to allow more than one unit to overlap with others in the range over which they are not at full power thereby averaging the unit nonlinearity, as illustrated in Fig. 8.8. The solid line with square plotted in Fig. 8.7 corresponds the IMD_3 product with the overlapping technique.

To understand the effectiveness of the segmented power generation scheme and the overlapping technique more clearly, error vector magnitude (EVM) of an

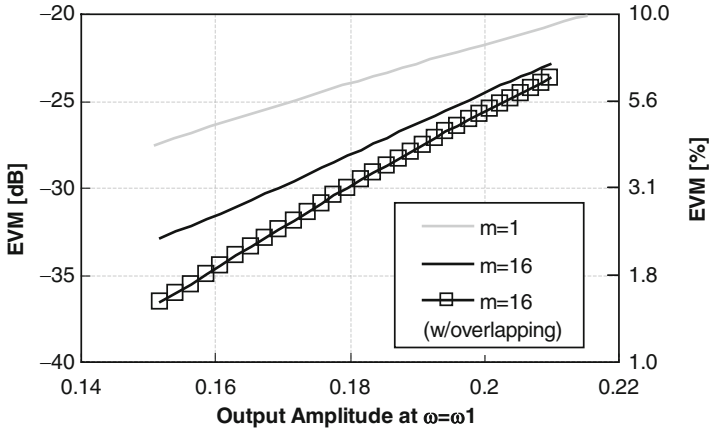

Fig. 8.9 Calculated EVM for an ideal OFDM signal

ideal orthogonal frequency division multiplex (OFDM) signal is calculated using following equation.

$$\mathrm{EVM} = \frac{\int \rho(\mathrm{A}_{in}) \bullet \mathrm{A}_{out}(\mathrm{A}_{in})|_{\omega=2\omega_1-\omega_2}\, d\mathrm{A}_{in}}{\int \rho(\mathrm{A}_{in}) \bullet \mathrm{A}_{out}(\mathrm{A}_{in})|_{\omega=\omega_1}\, d\mathrm{A}_{in}} \tag{8.9}$$

Where $\rho(\mathrm{A}_{in})$ is the probability density function of the input signal in amplitude, and $\mathrm{A}_{out}(\mathrm{A}_{in})|_{\omega=2\omega_1-\omega_2}$ and $\mathrm{A}_{out}(\mathrm{A}_{in})|_{\omega=\omega_1}$ are the output amplitude of the IMD_3 product and desired signal, respectively.

$$\begin{aligned} \mathrm{A}_{out}(\mathrm{A}_{in})|_{\omega=2\omega_1-\omega_2} &= |Y_m(\mathrm{A}_{in}(\cos\omega_1 t + \cos\omega_2 t)/2)|_{\omega=2\omega_1-\omega_2} \\ \mathrm{A}_{out}(\mathrm{A}_{in})|_{\omega=\omega_1} &= |Y_m(\mathrm{A}_{in}(\cos\omega_1 t + \cos\omega_2 t)/2)|_{\omega=\omega_1} \end{aligned} \tag{8.10}$$

Figure 8.9 shows the calculated result of EVM for three cases: (1) a conventional amplifier (m = 1), (2) segmented power generation scheme (m = 16), and (3) the segmented power generation scheme (m = 16) with the overlapping technique. The segmented power generation system and overlapping technique improve the EVM by 4.6 dB and 2.1 dB, respectively at an output amplitude of 0.17, where EVM of the conventional amplifier (m = 1) is about −25 dB (5.6%).

It should be noted that the linearity improvement due to the segmented power generation scheme is limited to input related non-linearity, such as transconductance and input capacitance non-linearity. Nonetheless, significant linearity improvement can be achieved since the input related non-linearity is generally dominant in a power generation circuit. Output related non-linearity, which is output impedance non-linearity, is usually smaller than the input related non-linearity due to the large input amplitude and small output load seen by an amplifier in a power generation circuit [7].

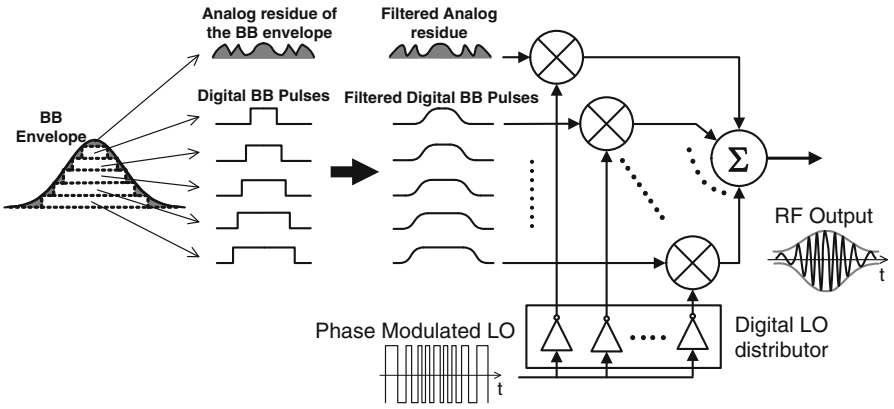

Fig. 8.10 The concept of power mixer input signal generation

8.2.3 Mixers as Power Generation Units

Despite benefits of back-off efficiency and linearity improvements in the segmented power generation scheme, there is a practical issue if the units were conventional RF amplifiers. Each power generation unit requires an RF input generation circuit. The amplitude of the RF input must be varied individually, while the phase must be precisely aligned. Also, the RF input signal generation circuits must be capable of well-controlled ramp-up and ramp-down to avoid spurious and sudden transient behavior, which add area and power overhead to the system. To circumvent this problem, power mixers are proposed as the power generation units [6]. The way phase modulated LO and BB signals are applied to power mixer units to generate a non-constant envelope RF signal is illustrated in Fig. 8.10. A BB envelope signal can be divided into several digital pulses and a residue part. The digital pulses can be filtered and pulse-shaped in baseband to avoid the spurious problems due to the quantization noise and aliasing signals. Identical phase modulated LO signals can be used to avoid the amplitude and phase mismatch issues of the RF input signal generation circuit. The LO signals are selectively applied to the power mixer unit via the digital LO distributor to dynamically shut-down unnecessary power mixer units. Then the pulses and the residue part are up-converted in frequency by the respective power mixer units, and a non-constant envelope RF signal is generated at the output of the power mixer array.

The pulse or the residue part can be easily generated by a DAC followed by a LPF. Furthermore, the DAC followed by a LPF can be shared by using a multiplexing network, as shown in Fig. 8.11. In our implementation a digital BB circuit controls the input of four DACs, such that two DAC (DA_0 and DA_2) followed by the LPF can generate time-varying BB signals, while remaining two DACs (DA_1 and DA_3) produce BB signals of a constant voltage. The digital BB circuit also controls the analog BB distributor so that the input of each power mixer unit is

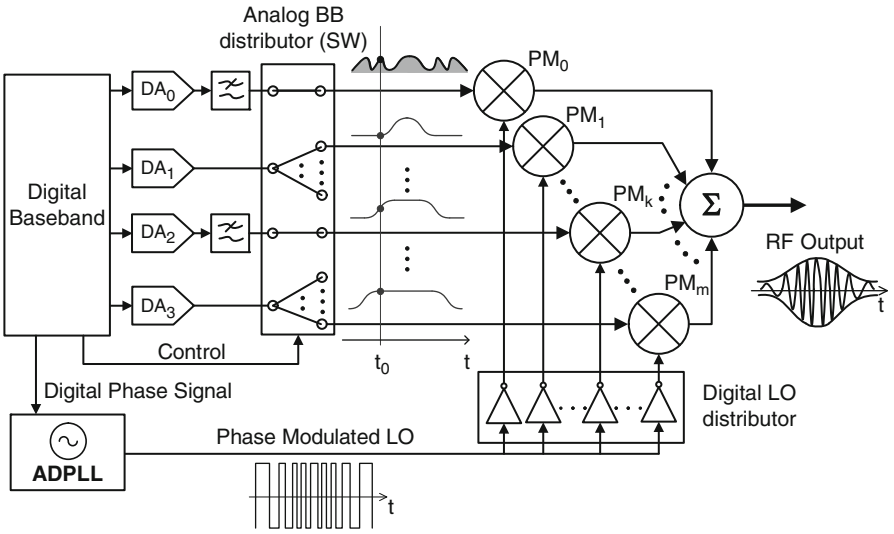

Fig. 8.11 Conceptual schematic of the BB input signal generation circuit

connected to one of the four BB signals. The input of the power mixer unit which corresponds to the residue part (PM_0) should always be connected to DA_0 followed by LPF, since it always operates at an intermediate power. The power mixer units which correspond to the BB pulses ($PM_1, PM_2, \ldots, PM_m$) are either completely on or completely off for most of the time. Therefore, these units are connected to the constant voltages (DA_1 and DA_3) for the most of the time. Only for the transition time, the time varying BB signal generated by the DA_2 followed by the LPF is applied to the power mixer unit. At $t = t_0$ for instance, power mixer units which produces the full power ($PM_{k+1}, PM_{k+2}, \ldots, PM_m$) should be connected to DA_3. The units which are turned off ($PM_1, PM_2, \ldots, PM_{k-1}$) should be connected to DA_1. The unit which is at transition (PM_k, where $1 < k < m$) is connected to DA_2 followed by the LPF. As a result, two BB circuits (a DAC followed by a LPF), two constant voltages, and a multiplexing network are sufficient for the BB input signal generation, regardless of the number of the power mixer units. It should be noted that the overlapping technique outlined in the previous section is utilized in the schematic of Fig. 8.11, since two power mixer units (PM_0 and PM_k) operate at intermediate power at the same time.

There are three things to be discussed in the actual implementation of the power mixer array. First, the power mixer array is compatible with a CMOS process, since MOS transistors make good switches. Second, the input of the DAC should be oversampled such that a BB envelope signal can be divided into pulses and a residue correctly. The sampling frequency should be m times higher than that of a conventional envelope restoration system. Also, the control frequency of the analog BB distributor and the digital LO distributor should be m times higher

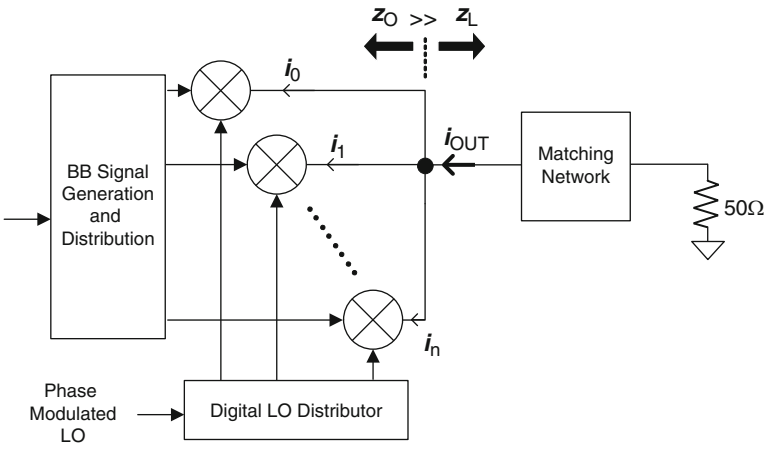

Fig. 8.12 Current domain signal combination at the output of the power mixer

than the envelope bandwidth. On the other hand, the required dynamic range is relaxed by a factor of $20\log_{10}(m)$ dB, which implies the required effective number of bits for each DAC is lower by $\log_2(m)$ bits. This is because the number of the operating power mixer units effectively represents the $\log_2(m)$ MSB of the BB envelope signal digital-to-analog conversion. Finally, mismatch between the power mixer units should be addressed. Since each power mixer unit represents the LSB side of the dynamic range, the mismatch requirement can be relaxed. Fortunately with a careful layout and routing, the mismatch does not affect the overall system performance.

8.2.4 Signal Combing at the Output Network

Another advantage of the power mixer array approach is the ease with which signal combining can be performed using a linear signal combination in the current domain, as shown in Fig. 8.12. To obtain a high peak power, the output matching network should be designed such that the output load seen by the power mixer array (Z_L) is small enough. Typically, Z_L is about 5Ω or smaller for a CMOS watt-level power generation circuit simply based on the reliability issues associated with maximum allowed voltage swing experienced by the output transistors. In contrast, the output impedance of the power mixer array (Z_O) should be much larger than Z_L (typically around 50Ω) to guarantee high efficiency. Then the power mixer units act as ideal RF current sources, and the linear current summation is achieved regardless of the number of the activated power mixer unit.

8.2.5 Digital LO Amplification Versus Conventional Analog Driver Amplifiers

Another important advantage of the polar architecture for high-power generation in a scaled CMOS technology is the digital LO amplification, in which LO signal is amplified using inverters as we have discussed in Sect. 8.1. It can eliminate the large and flexible matching networks of conventional analog driver amplifiers, and take advantage of fast and power efficient thin oxide devices. This section compares power and area efficiencies between the digital LO amplifier (e.g. inverters) and conventional analog driver amplifiers.

To drive a PA having an input capacitance C_{PA} by inverters, the power consumption of the preceding driver stage is approximately expressed as [8]

$$P_D = fC_{PA}V_{DDL} \tag{8.11}$$

where V_{DDL} is the supply voltage for the inverters.

Taking into account that the power is also consumed by the chain of the driver stages, whose gate widths are designed proportional to the preceding stages, total power consumption of the entire driver stages can be expressed as

$$P_D = \alpha\omega C_{PA}V_{DDL}^2\,(r/r-1) \tag{8.12}$$

where the gate width is r times larger than the preceding stage. Although α is theoretically equal to $1/2\pi$ from Eq. (8.11), there are some non ideal effects, such as drain capacitance of the driver stage, mirror capacitance, and power consumption by the short circuit [9]. In reality, it tunes out that α is around 1/5 with r of 3, as it is simulated with different CMOS technologies.

Total power consumption of the conventional analog driver stages to generate the output swing of V_A can be expressed as

$$P_{Conv} = V_A^2/(2R_L\eta) \tag{8.13}$$

where η and R_L are the power added efficiency (PAE) of the driver stages and load impedance, respectively. The load impedance R_L can be expressed by the load capacitance of the PA and quality factor of the matching circuit as,

$$R_L = Q/(\omega C_{PA}) \tag{8.14}$$

By substituting Eq. (8.14) into Eq. (8.13), we obtain

$$P_{Conv} = \omega C_{PA}V_A^2/(2Q\eta) \tag{8.15}$$

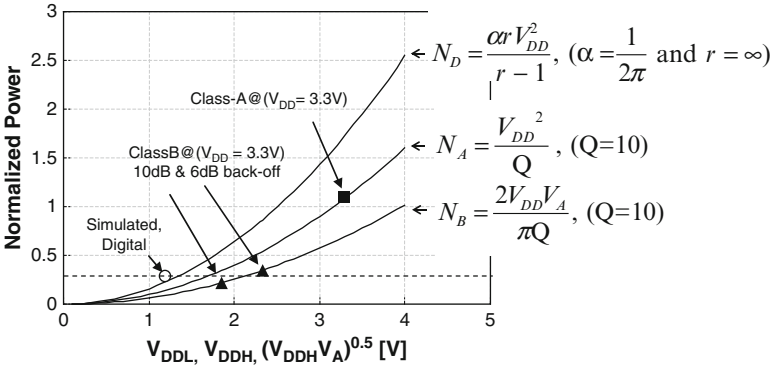

Fig. 8.13 Normalized power consumption for digital, class-A and class-B based driver stages

It is useful to calculate the power consumptions for ideal class-A and class-B driver stages to know practical and ideal cases, respectively. For class-A amplifiers, as the maximum efficiency is equal to $(V_A/V_{DDH})^2/2$, Eq. (8.13) can be rewritten as

$$P_A = \omega C_{PA} V_{DDH}^2 / Q \tag{8.16}$$

where V_{DDH} is the supply voltage for analog amplifiers. For class-B amplifiers, Eq. (8.15) can be rewritten as,

$$P_B = 2\omega C_{PA} V_{DDH} V_A / (\pi Q) \tag{8.17}$$

Note that the Eqs. (8.13), (8.16), (8.17) have quite similar dependencies, as all are proportional to the frequency, load capacitance, and square of the voltage. We define normalized power consumption in terms of capacitance and frequency, to compare the power consumption of digital and analog driver stages as,

$$N = P/\omega C_{PA}. \tag{8.18}$$

Then, the power efficiency for the digital, class-A, class-B amplifiers are expressed as,

$$N_D = \alpha {V_{DD}}^2 (r/r-1) \tag{8.19}$$

$$N_A = {V_{DDH}}^2 / Q \tag{8.20}$$

$$N_B = 2V_{DDH} V_A / (\pi Q). \tag{8.21}$$

The normalized power consumptions for ideal digital, class-A, and class-B amplifiers are plotted in Fig. 8.13. Solid lines represent calculated curves of Eq. (8.19),

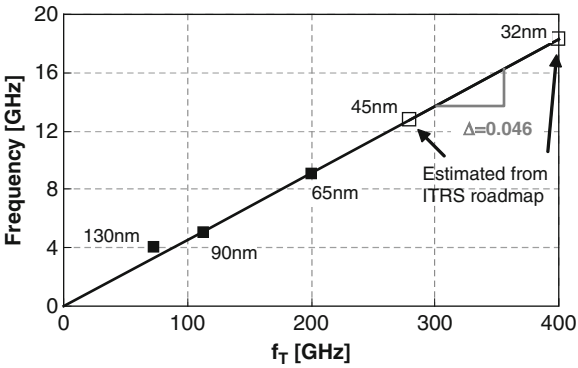

Fig. 8.14 The relation between f_T and frequency where the inverter chain can amplify signal

(8.20), and (8.21). Q of 10 is used for the class-A and class-B analog amplifiers, and r of infinity and α of $1/2\pi$ are used for the digital amplifiers. Note that the power consumption of class-A and digital driver stages does not depend on back-offs. The solid square represents the normalized power consumptions with V_{DDH} of 3.3 V. For class-B amplifiers, normalized power efficiency with 6dB and 10dB back-offs, as they are typical numbers for analog driver stages to deal with WCDMA and OFDM standard, respectively, are plotted with solid triangles. The circle corresponds to the simulated normalized power consumption of a digital amplifier with r of 3 and V_{DDL} of 1.2. It is almost on the calculated curve, showing non-ideal effects are negligible. It can be seen that the digital amplification can take advantage of the low supply voltages of the logic transistors and has much smaller power consumption than class-A driver stages, which are practical analog implementation, and achieves comparable efficiency to class-B power amplifiers, which corresponds potential limit for analog implementations.

The simulation results of maximum frequency where an inverter chain can amplify signal with r of 3 is shown in Fig. 8.14. The frequency for 45 nm and 32 nm CMOS technologies are estimated from ITRS roadmap and also shown in the figure. The frequency is proportional to the unity gain frequency, f_T, and is about 4.6% of the f_T. In reality we have to consider process-voltage-temperature (PVT) variation, 50%–60% of the simulated frequency shown in Fig. 8.14 will be the upper limit of the operating frequency.

8.3 Implementation and Circuit Details

8.3.1 Architecture Overview

The system block diagram of implemented power mixer array is shown in Fig. 8.15. In this implementation, the output currents of power mixer units are combined at their outputs, where the non-constant envelope RF signal is created. The resultant

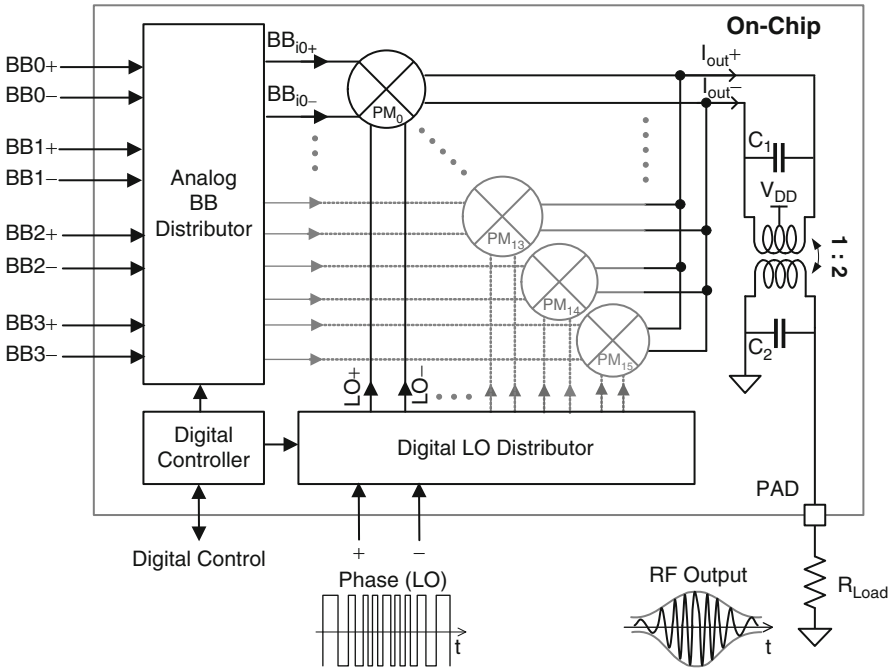

Fig. 8.15 Complete system block diagram of the implemented power mixer array system

non-constant envelope differential current is impedance transformed to drive the external single-ended 50Ω load using an on-chip transformer. Sixteen power mixer units are implemented to guarantee that (1) back-off efficiency dependence is almost the same as that of a class-B power amplifier, (2) linearity is improved, (3) required oversampling ratio is not very high, and (4) overhead in the layout to maintain the matching and minimizing the skew is negligible. The differential phase modulated LO signal is buffered and selectively applied to the desired number of power mixer units by the digital LO distributor. The choice of how many and which power mixer units receive the LO is controlled by an on-chip digital controller. The differential BB envelope signal is applied to the power mixer units via an analog BB distributor, which connects each power mixer unit to any four of the differential BB input signals.

A prototype was fabricated in a standard 130 nm CMOS process. The entire chip occupies a small area of 1.6 mm by 1.6 mm (shown in Fig. 8.20b). Phase modulated LO and BB signals are provided by an external signal generator and external DACs with LPFs, respectively. The DACs as well as the on-chip digital controller is controlled by a FPGA board.

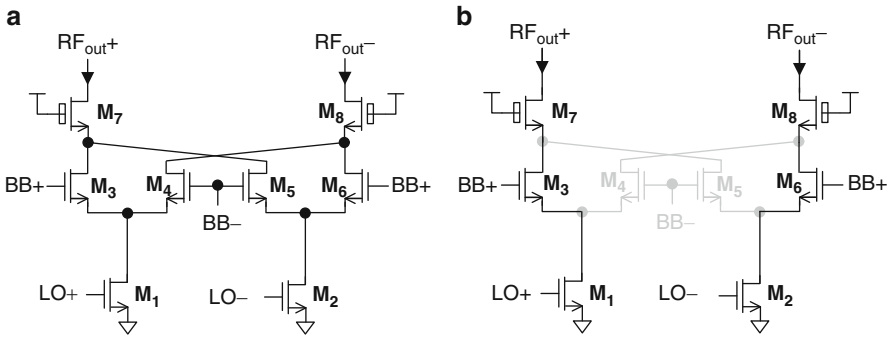

Fig. 8.16 (**a**) The schematic of the power mixer unit, (**b**) The schematic of the power mixer unit in the extreme case, with very large

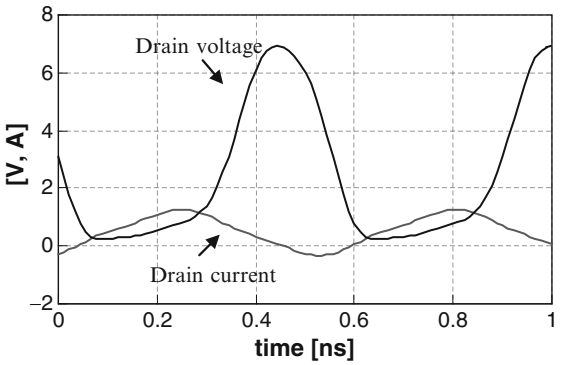

Fig. 8.17 The simulated drain voltage and total current of the power mixer array in the extreme case

8.3.2 Power Mixer Unit

The schematic of the power mixer unit is shown in Fig. 8.16a. The power mixer has high peak power efficiency, since the lower-tree common-source transistors driven by the LO switch between triode and cut-off modes. The BB signals are applied to the middle-tree differential pairs (M_3, M_4, M_5, and M_6). The differential pairs work as a cascode for the LO signals, and the power mixer employs another cascode with thick-gate-oxide top transistors (M_7 and M_8) to increase the maximum drain voltage swings without raising reliability issues, and to boost the output impedance.

To understand the power efficient operation of the power mixer, an equivalent circuit in the limiting case, where the BB+ input signals is very high and the BB- input signal is very low, is shown in Fig. 8.16b. In this limiting case, the cross coupled paths can be neglected and the amplifier operates exactly the same as the switching amplifier. The simulated drain voltage and current waveforms of Fig. 8.17

show the switching operation of the power mixer, which enables a peak drain efficiency of 60% with an output power of +32 dBm (1.6 W) at 1.8 GHz with sixteen power mixer units. It draws 0.88 A from a 3 V supply in the simulation. Note that the linearity of the power mixer unit, or differential pair, does not affect the overall linearity, as discussed in Sect. 8.2.4.

8.3.3 Output Impedance Matching Network

An Output impedance matching network is designed using a transformer and a capacitor. Transformer is suitable for a watt-level power generation circuit, since it is wideband and can have smaller loss than LC matching network when the output network is implemented on chip, where the Q of on-chip inductors can not be very large [10]. It can also converts a differential input signal to a single-ended output signal. In our design, the numbers of the primary turn and secondary turn are one and two, respectively. In the ideal transformer with a coupling coefficient of one, 50Ω load is transformed to 12.5Ω differential load, and single-ended power mixer array sees a small load of 6.25Ω In this implementation, single-ended power mixer array sees a 3.6Ω purely resistive load at 2.0 GHz with the drain capacitance (C_d), bonding wire inductance (L_{bond}), leakage inductance and parasitic capacitance of the transformer (T_1). In the layout, the length of the wires form each power mixer unit to the transformer is equal to match the delay between each unit. Simulated passive efficiency of the output matching network is about 80%.

8.3.4 Digital LO Distributor

The single-ended version of the digital LO distributor is shown in Fig. 8.18. It has a tree structure to match the delay for each path. The NOR gates drive the common-source transistors of the power mixer core (M_1 and M_2 in Fig. 8.16) with a 1.2 V square wave. To guarantee the differential balance, buffers are implemented by inverters and nor-gates with cross-coupled inverters (not shown in the figure). The NOR gates are used to improve the back-off efficiency of the digital LO distributor as well as power mixer array, since the output of a NOR-gate can be pulled down to corresponding power mixer unit, individually and dynamically.

The area of driver amplifiers with matching network, if any, is compared with published CMOS PAs, where driver amplifier is integrated without off-chip matching network. CMOS PAs with similar output power, which is from +30 to +33 dBm, are chosen for the comparison. Figure 8.19 shows the die micrographs with driver and matching network [10–13]. It can be seen that drivers with matching networks occupy large amount of die area. Die micrographs of PAs without matching network are shown in Fig. 8.20 [14]. Only small portions of the die are

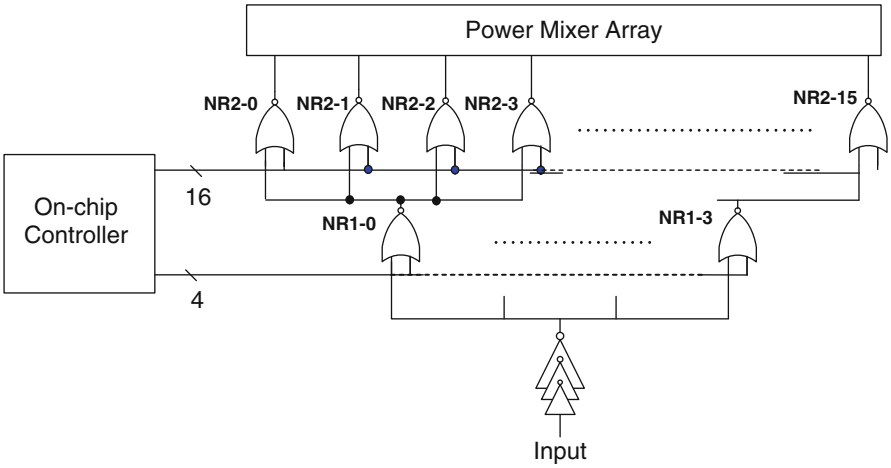

Fig. 8.18 The LO digital distributor

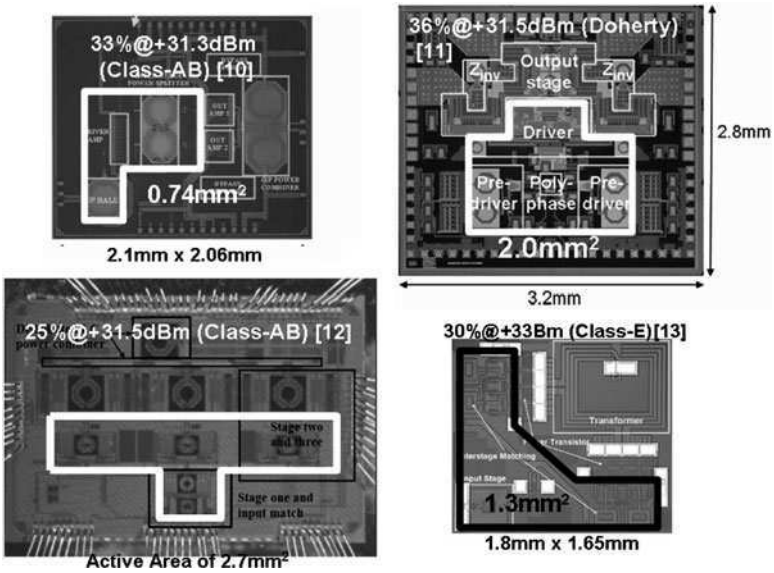

Fig. 8.19 Die micrographs of CMOS PA with driver and matching network, and output power from +30 to +33 dBm

occupied by the driver amplifier. The die micrographs shown in Figs. 8.19 and 8.20 have the same scales for comparison. It can be observed that the area overhead is very large. The reason could be to layout the matching network symmetrically with avoiding unwanted couplings. The result of the comparison is summarized in Table 8.1, clearly showing the advantage of the inverter-based driver stages.

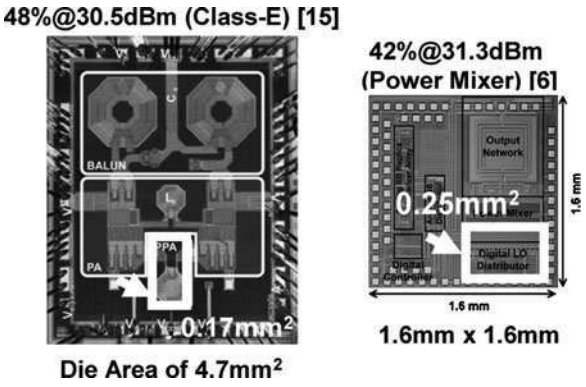

Fig. 8.20 Die micrographs of CMOS PA with driver and without inter-stage matching network

Table 8.1 Occupied area comparison with CMOS PAs with driver amplifiers

	Tech.	Chip area	Driver occupied area[a]	PAE	P_{SAT}	Freq.	Inter-stage transformer or inductor	Topology
	–	mm^2	mm^2	%	dBm	GHz	–	–
[11]	90 nm	4.3	0.74	33	31.3	2.4	Yes	Class-AB
[12]	65 nm	2.7[b]	–	25	31.5	2.4	Yes	Class-AB
[13]	130 nm	9.0	2.0	36	31.5	1.75	Yes	Doherty
[14]	180 nm	3[c]	1.3	31	33.0	1.8	Yes	Class-E
[15]	130 nm	4.7	0.17	48	30.5	1.7	No	Class-E
[6]	130 nm	2.6	0.25	42	31.3	1.8	No	Power Mixer

[a]Area with inter-stage matching circuit
[b]Active area
[c]Without bonding pads

8.3.5 Analog BB Distributor and Controller

The analog BB distributor depicted in Fig. 8.15 consists of thirty-two, one-to-four, analog multiplexers. One of the four differential BB inputs is applied to the power mixer unit. Four 16bit shift registers are implemented to control the state of the analog BB distributor and the digital LO distributor. The same number of latches as registers is also implemented so that the output of the on-chip controller is updated all at once. 3 V and 1.2 V supply are used for the analog BB distributor and controller, respectively.

8.4 Measurement Results

Figure 8.21 shows the measured frequency response of maximum CW output power and peak PAE of the power mixer array, with an LO input power of +3 dBm.

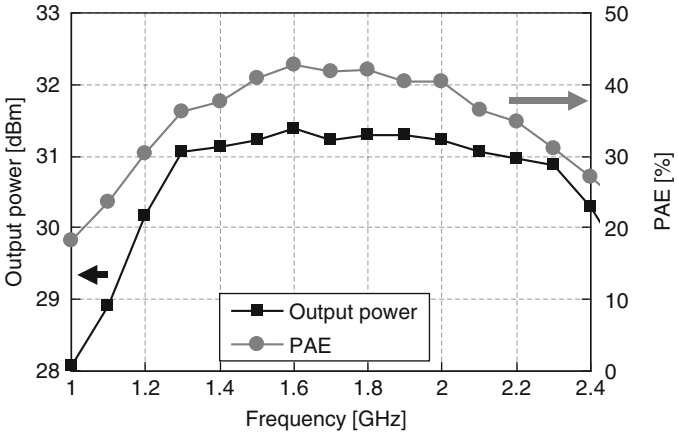

Fig. 8.21 Measured frequency response of output power and PAE

It should be noted that PAE of the power mixer array, which subsumes the driver amplifiers, includes DC power consumption of all the circuit blocks on-chip as,

$$\text{PAE} = \frac{\text{Output RF power–LO input power}}{\text{DC power consumption of the entire chip}} \tag{8.22}$$

The PAE is larger than 40% between 1.6 and 2 GHz with a peak of 43% at 1.6 GHz, and the output power is larger than 1 W over an octave range from 1.2 to 2.4 GHz. This broadband performance can be attributed to the high coupling coefficient ($k \sim 0.8$) of the on-chip transformer. The peak PAE and drain efficiency at 1.8 GHz is 42% and 46%, respectively. Without the on-chip transformer, the peak drain efficiency is estimated as 62%. This agrees with the simulation result in the Sect. 8.3.2. The power mixer array has an LO-to-RF power gain of 28.4 dB. It produces the maximum output power of 31.4 dBm with a BB input voltage of 450 mV at 1.6 GHz.

Figure 8.22 shows the measured PAE and normalized conversion gain versus the output power at 1.8 GHz. There are ripples when the output power is small as expected, and the ripple gets smaller with larger output power. It is almost negligible for the output power of greater than 20 dBm where gain flatness is important for a good EVM and output spectrum. output 1 dB compression point (P_{1dB}) is about 28 dBm.

Linearity robustness to the common mode voltage of BB signal should be discussed, since it varies due to the large PVT variations in a CMOS process. Figure 8.23 shows the conversion gains with different common mode voltages, V_{CM}. As we discussed in Sect. 8.2.2 the ripples at lower power output in the conversion gain have a limited impact to the overall linearity of the system.

The power mixer array is tested with a 16QAM modulated signal, which has non-constant envelope. Figure 8.24 shows the EVM and PAE dependence on the

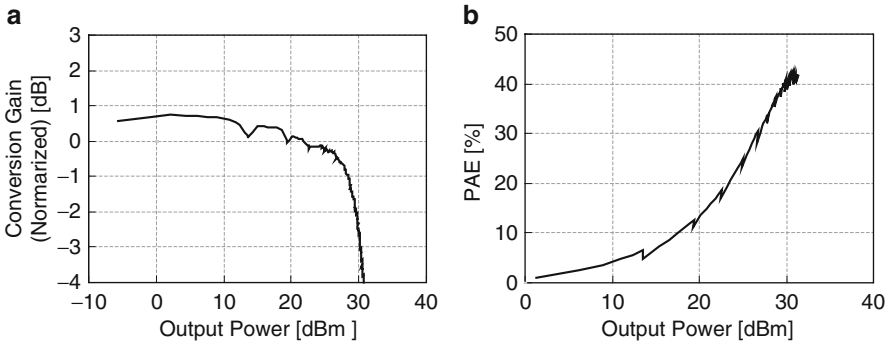

Fig. 8.22 Measured (**a**) Conversion gain and (**b**) PAE

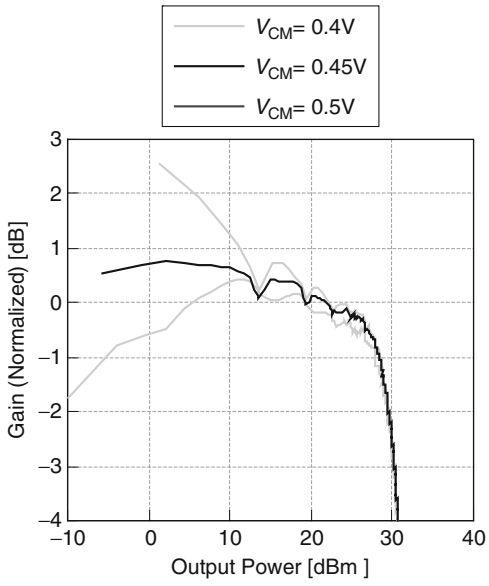

Fig. 8.23 Measured Conversion gain dependence of the common-mode bias

average output power. In this figure, the symbol rate is 50 kSym/s and the filter used for the BB pulse shaping is root-raised cosine with an excess ratio of 0.5. Output power of 26.4 dBm is achieved with EVM of 4.5%. EVM reaches below 1% with output power of less than 21.2 dBm. This indicates the ripple of the conversion gain has negligible impact to overall linearity performance. Measured spectrum and constellations are shown in Fig. 8.25.

The accurate processing of the baseband pulses and especially analog residue signal described in Fig. 8.10 is important to avoid the quantization noise and aliasing issues. The wideband output spectrum with a 16QAM signal is measured and compared with a calculated spectrum without either analog residue signal or external LPF, as shown in Fig. 8.26. The clock frequency of DACs used for both

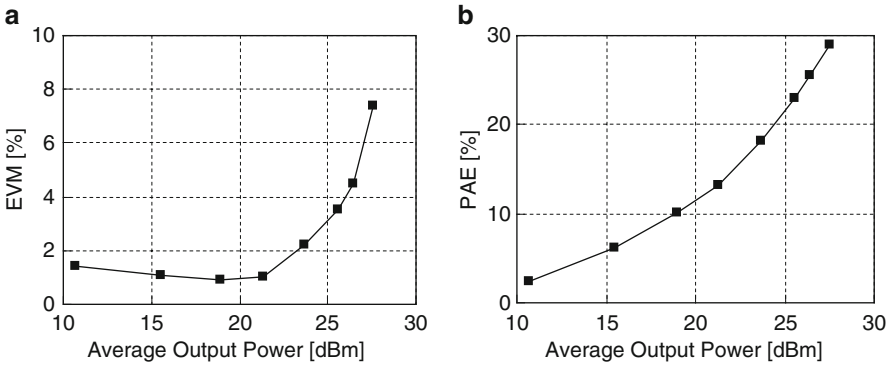

Fig. 8.24 Measured (**a**) EVM and (**b**) PAE with 16QAM signal

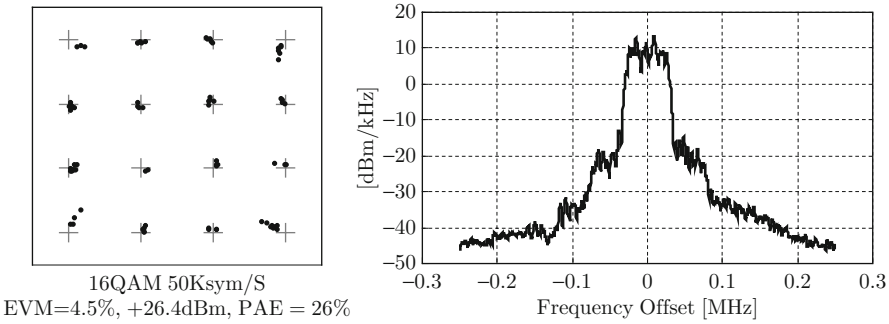

Fig. 8.25 Measured output spectrum and constellation

the measurement and calculations is 10 MHz, and an ideal sample-and-hold DAC outputs are assumed for the calculation. While strong aliasing signals with 10 MHz separation are observed with the calculated spectrum, no aliasing signal observed with the measured spectrum. Spurs at 20 MHz offset in the measured spectrum is maybe due to the test setup, where 20 MHz control signals are applied from a separate FPGA board to the on-chip digital controller with noisy wires. The effect of the analog residue signal on the quantization noise is also measured. Figure 8.27 shows the output spectrum with $\pi/4-$OQPSK modulation. Unwanted quantization noise is avoided by applying analog residue signal of the BB envelope to one unit. Although the clock frequency of the DAC for the analog baseband signal generation is 2 MHz in this measurement setup, the bandwidth can be extended when the digital baseband circuit is implemented on-chip.

As we discussed in Sect. 8.1, one of the major challenges in the conventional digital polar system is its limited output power range. Even in a conventional IQ transmitter system, an expensive and power consuming RF gain control circuit is required to realize large output power range. The power mixer array can provide

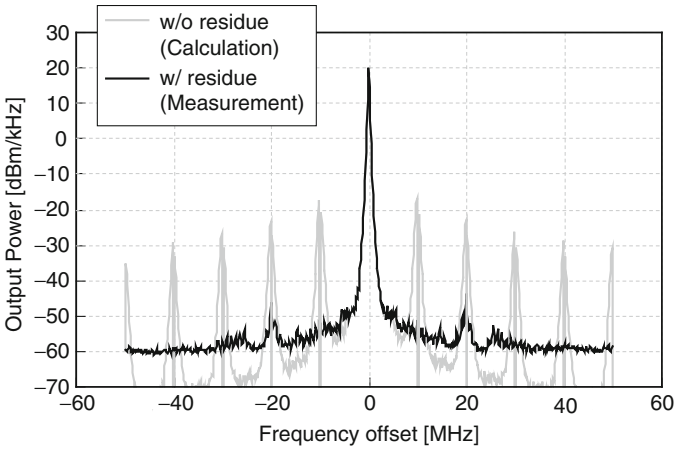

Fig. 8.26 The wideband spectrum with 16QAM modulation

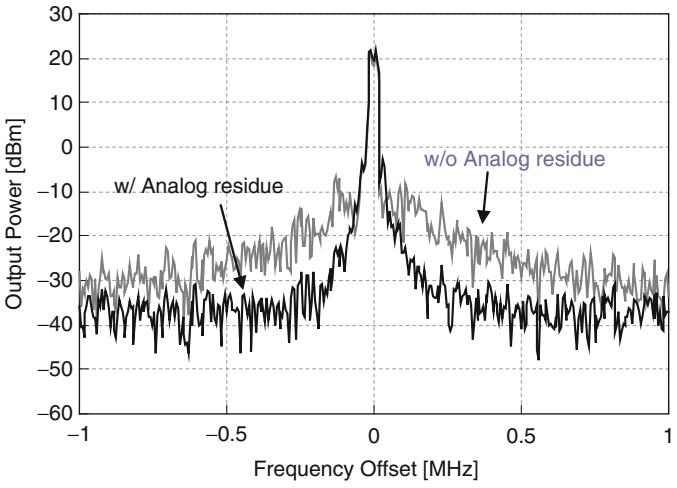

Fig. 8.27 Quantization noise suppression due to the analog reside signal

very small output power without any RF gain control circuit, since small LO leakage can be expected due to its double-balanced topology. To reduce the LO leakage, only one power mixer unit is activated and v_{cm} is set to 200 mV, which substantially reduces the transconductance of the switching stage. The LO leakage at the output is measured as −70 dBm without adjusting the DC offset of the baseband differential pairs. It can be further reduced by input offset cancellation techniques as evident from its reduction to lower than −91 dBm, when −0.82 mV differential DC input is applied to cancel the offset of the differential pair. The EVM with 16QAM signal is measured with large output power range, as shown in Fig. 8.28. It is less than 5%

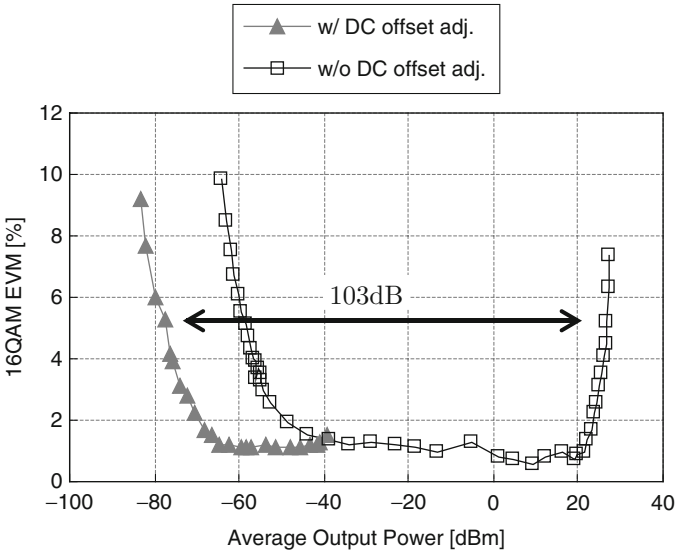

Fig. 8.28 Measured LO leakage dependence of the input DC offset voltage

for output power levels greater than −57.9 dBm without the adjustment. With the adjustment, EVM is less than 5% with output power levels greater than −76.2 dBm, and more than 100 dB output power range is achieved without any RF gain control circuit.

8.5 Conclusion

A new system and circuits in a CMOS process for an SDR transmitter was presented. Power mixer array offers required flexibility as the array can be controlled digitally and it does not require conventional analog driver stages with matching networks, while it does not create quantization noise or aliasing signals. It also takes advantage of a scaled CMOS technology and can achieve high power efficiency, since the power mixer works as a switching amplifier and area and power efficient digital driver amplifiers are employed. Test chip is fabricated in a CMOS technology and its effectiveness and suitability for an SDR transmitter are verified with measurement results.

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Index

A
Adaptive filter. *See* Adaptive interference cancelling (AIC)
Adaptive interference cancelling (AIC), 117, 118, 125, 126, 128–130, 133, 139–142
ADC. *See* Analog-to-digital converter (ADC)
Aliasing, 66, 69, 73
Aliasing signal, 187, 194, 199, 212, 214
All-digital transmitter, 55–62
Amplitude control word (ACW), 55
Analog baseband (ABB), 151–168
Analog-to-digital converter (ADC), 4, 8, 25–27, 31, 35, 48, 86, 171–175
  continuous-time (CT) delta-sigma, 178
  delta-sigma, 175–187
  discrete-time (DT) delta-sigma, 178
  pipeline, 175, 176
  successive approximation (SAR), 175–176
Analog two-stage polyphase harmonic rejection (HR), 121–125
Anti-aliasing, 86, 88–91, 93, 96, 99, 110

B
Back-off, 194, 199, 204, 205, 207
Balun, 8, 13, 21, 22, 29, 30, 131, 135, 136
  on-chip, 21, 31
Baseband-WIS (Windowed integration sampler), 90–91
BAW. *See* Bulk acoustic wave (BAW)
BB envelope signal, 193, 199–201, 205
Bill of material (BoM), 4, 18
Bit error rate (BER), 174, 175
Blocker, 174, 175
Bulk acoustic wave (BAW), 114
Butterworth, 164–166, 168, 172, 173

C
CDMA, 97
Charge-sharing, 101, 103
Chebyshev, 165, 168
Clock symbol (CKS) oversampling, 60, 61
Clock variable (CKV), 49, 50, 53–55, 59–62
CMOS, 3–31, 37–44, 48, 52, 53, 55, 59, 63, 79, 85, 109, 110, 113–115, 118, 130, 135
  nanometer-scale, 39–41, 55
  PA, 207–209
  scaling, 43
Cognitive radio (CR), 113, 115
Cross layer optimization, 5
Cut-off frequency, 151, 159, 160, 164, 165, 168

D
DAC. *See* Digital-to-analog converter (DAC)
Decimation, 63, 64, 66, 68, 69
Delta-sigma dithering, 36, 43, 48, 53
DFC. *See* Digital-to-frequency converter (DFC)
Digital baseband (DBB), 35, 41, 43–46, 55, 60, 62
Digital LO distributor, 199, 200, 205, 207–209
Digitally-assisted RF, 35–80
Digitally-controlled crystal oscillator (DCXO), 44, 47
Digitally-controlled oscillator (DCO), 45–47, 49–62, 78–80
Digitally-controlled oscillator (DCO) gain estimation, 51
Digital power amplifier (DPA), 55–57, 60, 61, 78
Digital RF, 35–80

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Digital signal processing (DSP), 44, 86, 91, 94–96
Digital-to-analog converter (DAC), 35, 48, 55, 56, 171, 176, 178, 182, 183, 185–188, 199–201, 212
  RF, 55–57
Digital-to-frequency converter (DFC), 55–57, 59, 60
Digital-to-RF amplitude converter (DRAC), 1, 55, 56
Direct conversion, 87–88, 92, 152
Discrete-time
  pole, 100
  receiver, 63–77, 79
Distortion dependence shaping, 196
DRAC. *See* Digital-to-RF amplitude converter (DRAC)
Driver, 193, 202–204, 207–210, 214
Duty-cycle, 154–159, 163–164, 168
DVB-H, 27, 172, 173
Dynamic element matching (DEM), 182

E
EDGE, 27, 29, 30, 44, 45, 56, 58, 60, 61, 172
Efficiency, 191–194, 201, 203, 204, 206, 210, 214
  back-off, 194, 199, 205, 207
  power-added (PAE), 202, 209–211
Elliptic, 159, 165, 168
Equalizer, 125–127, 129
Error vector magnitude (EVM), 197, 198, 210–214

F
FDD. *See* Frequency-division duplex (FDD)
Filter
  analog baseband, 93, 94
  antenna, 7
  anti-aliasing, 157–163, 172, 178, 179
  band select(ion), 88, 114, 116, 118
  channel select, 17, 19
  digital, 93
  discrete time, 152, 159, 168
  discrete-time analog decimation filter (DEDec), 96
  discrete-time FIR, 96, 101
  discrete-time IIR, 68, 71, 96, 99–102, 104
  DT low-pass, 152–154, 158–160, 163, 164, 166, 168
  external band-pass, 35
  finite impulse response (FIR), 127, 154, 159–163, 168
  Gm-C, 153
  infinite impulse response (IIR), 51, 63, 67–71, 73–75
  low-pass (LPF), 8, 19–21, 23, 24, 28, 35, 59, 113–147, 152, 156, 158–160, 165, 168, 199, 200, 205, 211
  passive low-pass, 152, 159, 160
  passive RC, 94, 96, 99
  poly-phase, 8
  reconfigurable, 151–168
  RF, 114, 117, 131
  RF preselect, 88–90, 93, 94, 110
Filtering
  anti-blocking, 93
  blocker, 117–121, 123, 133, 137–138
  channel selection, 93
  charge-domain discrete-time, 152
Flicker noise, 108, 152, 155, 156, 158, 159, 162, 166
1/f noise, 107, 108
Fractional-N, 36, 48, 60
Frequency
  command word (FCW), 48–50, 55, 56, 58–62, 77
  reference (FREF), 44, 48–51, 53–55, 57–62
Frequency-division duplex (FDD), 6, 8, 18, 21, 24, 31

G
Global Positioning System (GPS), 3, 27
GSM, 6, 27, 28, 36, 37, 41–46, 51, 56, 58, 64, 77, 78, 87, 91, 95, 96, 99, 100, 104, 110, 151, 152, 172

H
Harmonic rejection (HR), 113–147
  mixer, 117, 121, 122, 133, 139, 141, 142, 146, 147

I
IIP2. *See* Second order input interception point (IIP2)
IIP3. *See* Third order input interception point (IIP3)
Image rejection (IR), 88
Integral nonlinearity (INL), 196
Integrator, 176, 178, 179, 182, 183
Interference estimate, 117, 125–129, 133, 134, 140
Intermodulation, 196
Inter modulation distortion (IMD), 196–198
IQ transmitter, 191, 192, 212

J
Jitter, 178, 184–186

L
Least mean square (LMS) algorithm, 127, 130
Linearization, 116
LNTA. *See* Low noise transconductance amplifier (LNTA)
Local oscillator (LO), 36, 42–44, 47, 63, 64, 154, 191, 193, 199, 200, 202–209
  leakage, 213, 214
Long term evolution (LTE), 172
Loop filter, 37, 48, 51, 55, 58, 62
Low-IF, 44, 63, 64, 92
Low-noise amplifiers (LNA), 7, 12–13, 23, 24, 35, 63, 85, 94, 104–107, 110, 116, 118, 120, 141
  shunt-shunt feedback, 13
  wideband, 7
  wideband noise cancelling, 2
Low noise transconductance amplifier (LNTA), 44, 64, 67, 72, 120–123, 125, 127, 128, 130–132, 135, 136, 139, 144, 146
Low-pass filter (LPF)
  transimpedance (TI), 8, 19

M
Mismatch, 117, 122, 124, 125, 127, 129–132, 138, 140–142, 145, 152
Mixer
  harmonic rejection (HR), 117, 121, 122, 133, 139, 141, 142, 146, 147
  harmonic suppressing, 109
  multi-tap direct sampling (MTDSM), 63, 67, 70–73, 75–77
  passive, 8, 13–15, 31
  sampling, 18–21, 31
Moore's law, 37
Moving average (MA), 64–70, 73
Multiband receiver, 176
Multirate
  ADPLL, 57–62
  DFC, 59, 60
  frequency modulator, 57–62
Multi-standard, 171–188

N
Narrowband receiver, 116, 118, 121
Network on chip (NoC), 6
Noise, 115–118, 120, 121, 123, 130, 131, 133, 135, 136, 140
Noise figure (NF), 115–118
Noise power spectral density, 180
Nonlinearity, 114–117, 119, 121, 129, 136, 141

O
Op-amp (opamp), 153, 158
Orthogonal frequency domain multiplex (OFDM), 192, 198, 204
Out-of-band
  blocker, 7, 35
  emission, 194
  interference (OBI), 12, 114–119, 121, 135, 136, 141
  linearity, 15, 121
  noise, 8, 18, 19
  nonlinearity, 117, 141
Output impedance, 198, 201, 206, 207
Output matching, 201, 207
Output P_{1dB}, 210
Output power range, 193, 212–214
Oversampling, 175, 177, 179, 182–186

P
Phase-locked loop (PLL)
  all-digital, 43, 44, 47–55, 58, 79
  reconfigurable, 41
Phase modulated LO, 191, 193, 199, 205
PLL. *See* Phase-locked loop (PLL)
Polar, 36, 41, 43, 44, 55, 56, 59–62, 191, 192, 194, 202, 212
  digital, 35–80
Power amplifier (PA), 191, 194, 202, 204, 205
  class-AB, 191, 209
  class-B, 194, 203–205
  watt-level, 197, 199, 201, 203, 205, 207, 209
  class-E, 209
Power mixer
  array, 191–214
  unit, 193, 199–201, 204–207, 209, 213
Process-voltage-temperature (PVT), 50, 52, 61, 78, 96, 99, 100
Programmable gain amplifier (PGA), 95, 97, 151–154, 165–168
Pulling, 59, 61
Pulse generator, 153, 154, 163–164, 167, 168

Q
16QAM, 210–213
Quantization noise, 171, 174–177, 183, 186, 191, 192, 194, 199, 211–214
Quantizer, 176, 177, 179, 182

R
Reconfigurable, 41
Reconfigurable analog baseband, 151–168
Resolution of an ADC, 174
RF built-in self-test (RF-BIST), 45, 77–79

S
Sample rate conversion (SRC), 59, 61
Sampling
  direct RF, 63
  frequency, 172–176, 179, 181–188
  noise, 173, 183, 184, 186
SAW. *See* Surface acoustic wave (SAW)
SDR. *See* Software-defined radio (SDR)
Second order input interception point (IIP2), 14, 24, 25, 27, 114–116, 131
  calibration, 13–15, 24
  in-band, 136
  out-of-band, 136–137
Signal-to-noise ratio (SNR), 175–178, 180–187
Sinc, 87, 90, 96, 99, 101, 103
SoC. *See* System-on-chip (SoC)
Software-defined radio (SDR), 3–31, 85–111, 113, 114, 117, 118, 130, 151–153, 191–214
  baseband engine, 4, 5
  front-end, 3–6, 29
  low-power, 93–99
  platform, 3–31
  receiver, 3, 6, 7, 12–19, 23, 24, 27, 28
  RX, 85–88, 91–110
  transceiver, 3–31
  transmitter, 3, 6, 8, 18–22, 28, 29, 31
Subsampling, 63
Surface acoustic wave (SAW)
  filter, 18, 19, 114
  less, 18, 31, 121
Switched capacitor, 178
Switching amplifier, 191, 206, 214
System-on-chip (SoC), 4, 6, 38, 41, 45, 79
  nanoscale CMOS, 3–31

T
Third order input interception point (IIP3), 15, 27, 114–118, 120, 130, 136, 131, 141, 142
  in-band, 136
  out-of-band, 117, 136–137
Time-domain, 39, 40, 73, 79
Time-to-digital converter (TDC), 49, 53–55, 58, 62, 79
Transconductor, 100, 101, 103, 107, 108
  discrete time (DT), 152–168
Transformer, 205, 207, 209, 210
Transimpeadance amplifier (TIA), 15, 16, 24, 25, 120–123, 130, 132–133, 135, 136, 138, 144, 145
Tunability, 152, 157, 165, 166, 168

V
Variable gain amplifier (VGA), 172
Voltage-controlled oscillators (VCO), 6–11, 22, 23, 29, 30, 179, 187
  class-C, 9, 10

W
WCDMA, 27–30, 56, 151, 152, 172, 174, 175, 204
WiMAX, 27, 30
Windowed integration sampler (WIS), 88–90, 94, 96
  rectangular, 90
  RF, 85–110
Wireless local area networks (WLAN), 3, 27, 172, 173, 175

Z
Z-domain, 100, 101
Zero-IF, 6, 13, 44, 86, 87, 92, 118, 120